PRELIMINARY

INTEL Pentium® OverDrive® PROCESSOR

- **Powerful CPU Upgrade for Intel486™ CPU-Based Systems**
  - **— Makes Intel Procesor-Based Systems Run Faster**
  - **— Significantly Accelerates All Software Applications**
- **Designed for Systems Based on:**
  - **— Intel486™ SX Processors**
  - **— Intel486™ DX Processors**
  - **— IntelSX2™ Processors**
  - **— IntelDX2™ Processors**
- **Compatible with Installed Base of Thousands of Applications**
- **Based on Advanced Intel Pentium® Processor Technology**
- **Incorporates SMM Power Saving Features**

The Pentium® OverDrive® processor upgrades Intel486™ processor-based systems to Pentium processor technology. It features a true Pentium processor core (Superscalar Architecture, Branch Prediction, and faster floating point unit), silicon enhancements (separate code and data caches, 16 KB each, and 32-bit bus interface), and package innovations (on-package voltage regulation and fan heat sink).

290544-25

*Other brands and names are the property of their respective owner.

June 1995
Order Number: 290544-001

Intel Pentium® OverDrive® Processor

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This Specification should be used in conjunction with the *Intel486 Microprocessor Family Data Book* (Order Number 242202-002).

1.0 INTRODUCTION

This data sheet describes the Intel Pentium OverDrive processor, a CPU upgrade for most Intel486 SX, Intel486 DX, IntelSX2, and IntelDX2 processor-based systems. This processor upgrade will significantly accelerate all software applications run on your existing system, thereby increasing the overall performance of your PC.

It is important to note that this data sheet is intended to be used in conjunction with the *Intel486 Microprocessor Family Databook* (242202-002). Only information which is not in the databook will be included in this datasheet.

1.1 Pentium® OverDrive® Processor Product Overview

The Pentium OverDrive processor is the highest performance CPU upgrade available for systems based on the Intel486 family of CPUs. It brings Pentium processor technology (including Superscalar Architecture, Branch Prediction, faster floating-point unit, and separate data and code caches) to Intel486 processor-based systems.

Inclusion of the Pentium OverDrive processor socket in systems based on the Intel486 family of microprocessors provides the end user with an easy and cost-effective way to increase system performance. The majority of upgrade installations which take advantage of the Pentium OverDrive processor socket will be performed by end users and resellers. Therefore, it is important that the design be "end user easy", and that the amount of training and technical expertise required to install the OverDrive processors be minimized. Upgrade installation instructions should be clearly described in the system user's manual. In addition, by making installation simple and foolproof, PC manufacturers can reduce the risk of system damage, warranty claims and service calls. Feedback from Intel's upgrade customers highlight three main characteristics of end user easy designs: accessible socket location, clear indication of upgrade component orientation, and minimization of insertion force. Recommendations regarding designing for easy upgradability appear in Section 9.

1.2 Product Description

The Pentium OverDrive processor is designed to upgrade systems based on Intel486 SX, Intel486 DX, IntelSX2, and IntelDX2 processor-based systems and is based on Intel's Pentium processor technology. It is 100% binary compatible with the 8086/88, 80286, Intel386 DX, Intel386 SX, Intel486 DX, Intel486 SX, IntelSX2, and the IntelDX2 processor family.

The Pentium OverDrive processor provides significant improvements over the Intel486 CPU including:

- Superscalar Architecture
- Dynamic Branch Prediction
- Pipelined Floating-Point Unit
- Separate 16K Code and 16K Data Caches
- Improved Instruction Execution Times
- Write back MESI Protocol implemented in Data Cache
- System Management Mode

The Pentium OverDrive processor significantly increases the integer performance, and can attain up to 2x floating-point performance relative to an equivalent frequency IntelDX2 processor. The initial target bus frequencies for the Pentium OverDrive processor are 25 MHz and 33 MHz.

Figure 1-1 shows the Pentium OverDrive processor's two pipelines and floating-point unit that are capable of independent operation. Each pipeline issues frequently used instructions in a single clock. Together, the dual pipes can issue two integer instructions in one clock, or one floating point instruction (under certain circumstances, 2 floating point instructions) in one clock.

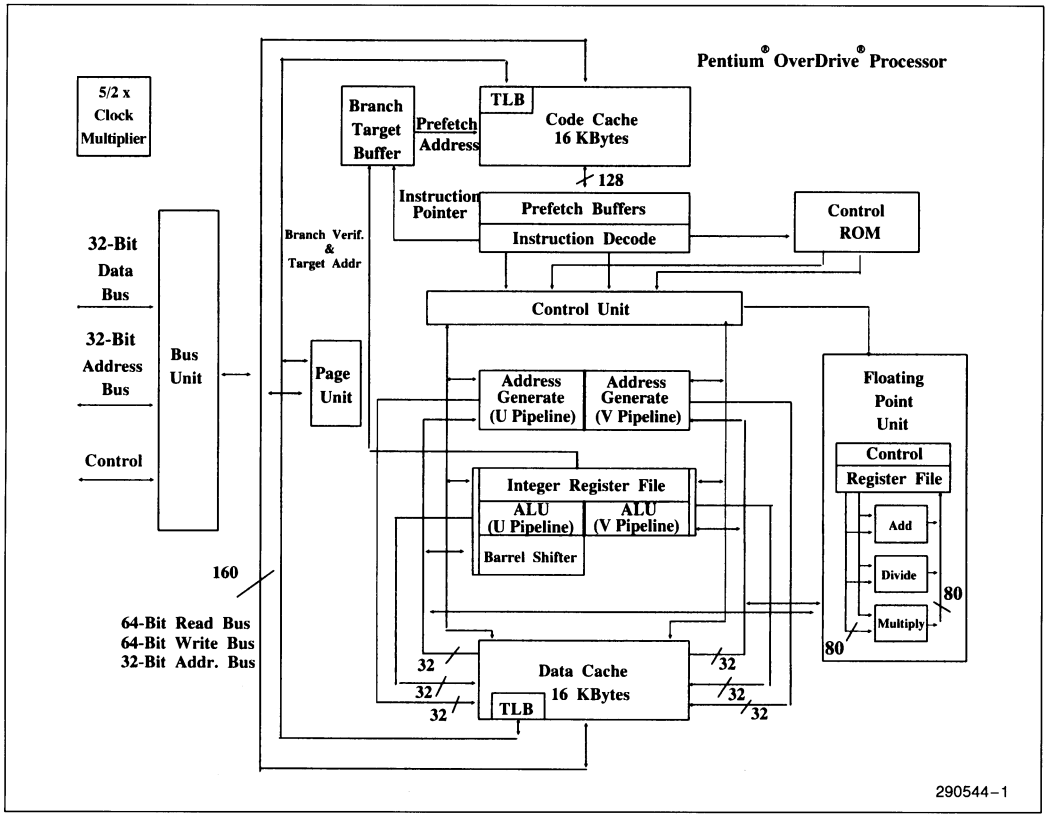


Figure 1-1. Pentium® OverDrive® Processor Block Diagram

The floating-point unit has been completely redesigned over the IntelDX2 processor. Faster algorithms provide at least 3X internal speed-up for common floating point operations including ADD, MUL, and LOAD. With instruction scheduling and overlapped (pipelined) execution, these three performance enhancements can allow many math intensive applications to achieve a 2X performance boost.

The Pentium OverDrive processor implements 32-bit address and data busses.

The block diagram shows that the Pentium OverDrive processor contains two instruction pipelines, the "u" pipe and the "v" pipe. Both the u- and the v-pipes execute integer instructions, while only the u-pipe executes floating point instructions. The one exception is the FXCH instruction which may also be executed in the v-pipe. Therefore, the Pentium OverDrive processor is capable of executing two integer instructions in each clock, or one floating point instruction in each clock. Floating point instructions can be paired in certain conditions(1). Each pipeline has its own address generation logic, arithmetic logic unit and data cache interface.

NOTE:

1. Refer to the *Pentium Processor Data Book* for more information on instruction execution timing and pairing.

Note that there are two separate caches, a code cache and a data cache. The data cache has three tag ports, one for each of the two pipes and one dedicated to handle snoops from other processors. It has a dedicated Translation Lookaside Buffer (TLB) to translate linear addresses to the physical addresses used by the data cache.

The code cache, branch target buffer and prefetch buffers are responsible for getting raw instructions into the execution units of the Pentium OverDrive processor. Instructions are fetched from the code cache or from the external bus. Branch addresses are remembered by the branch target buffer. The code cache TLB translates linear addresses to physical addresses used by the code cache.

The decode unit decodes the prefetched instructions so that the Pentium OverDrive processor can execute the instruction. The control ROM contains the microcode which controls the sequence of operations that must be performed to implement the Pentium OverDrive processor architecture. The control ROM unit has direct control over both pipelines.

1.3 Purpose of this Document

This document describes the system architecture and physical environment of the Pentium OverDrive processor. It also outlines differences between the Intel486 Family of processors and the Pentium OverDrive processor.

1.4 Compatibility Note

In this document, some register bits are shown as "Intel Reserved" (RES) and some pins are marked as "No Connects" (NC) or "Reserved" (RES). When reserved bits are called out, treat them as fully undefined. This is essential for software compatibility with future processors. When a pin is marked as a "NC" or "RES" it is important to not connect any other signals to such pins to ensure proper operation. Intel strongly recommends that you follow the guidelines below:

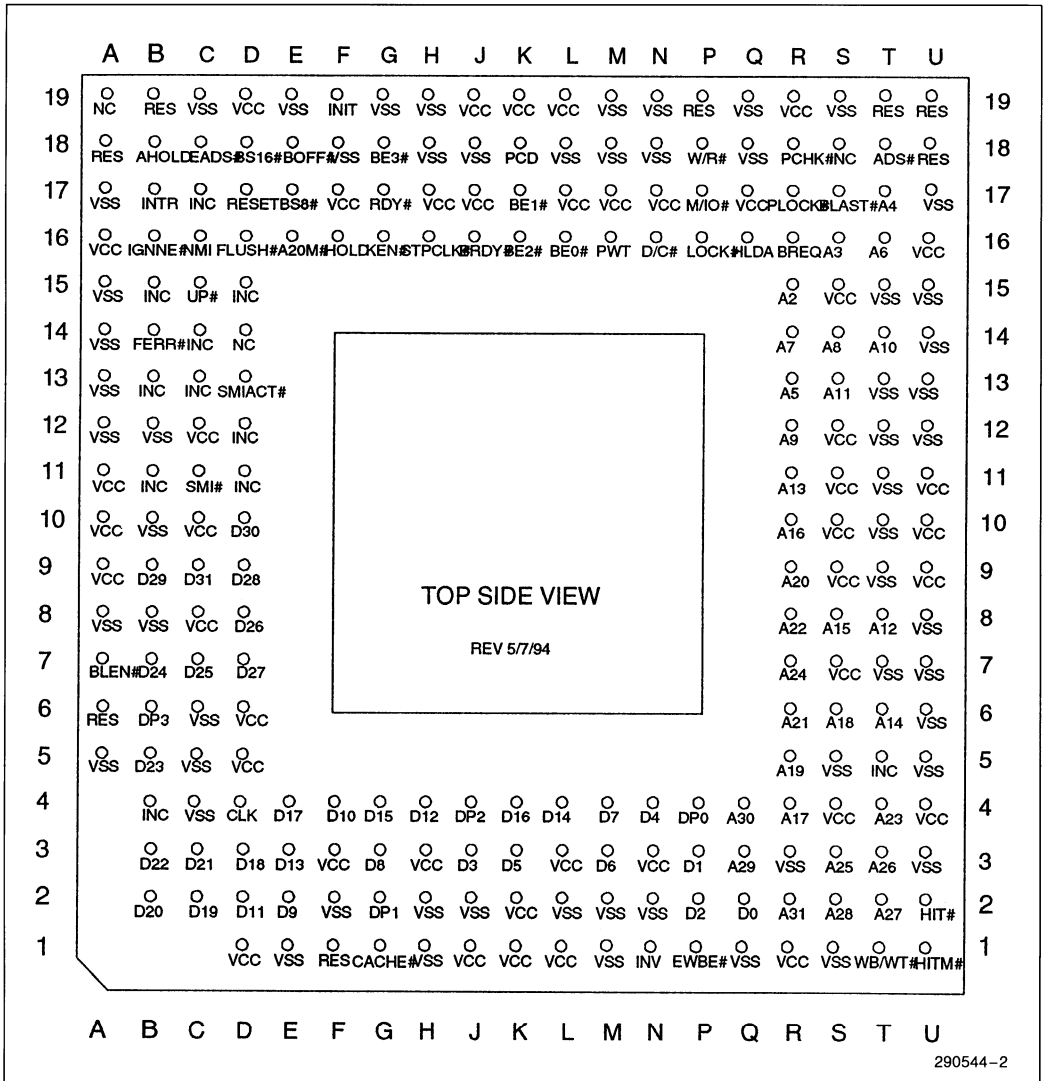
1) Do not depend on the states of any undefined bits when testing the values of defined register bits. Mask them out when testing.
2) Do not depend on the states of any undefined bits when storing them to memory or another register.
3) Do not depend on the ability to retain information written into any undefined bits.
4) When loading registers always load the undefined bits as zeros.
5) Never connect signals to device pins marked as "NC" or "RES"
6) **INC** Pins are defined as Internal No-Connects. This means that the pin is not connected to the processor internally. Since the pin is inert and floating, it may be used in any manner seen fit, but must meet the **INC** pin specifications. In general, all **INC** pins have an intended use to implement a single processor socket system design. The **INC** pin will never be used for any other function.

2.0 Pentium® OverDrive® PROCESSOR SPECIFICATIONS

The Intel Pentium OverDrive processor socket specifies 237 contacts. The 237 contacts correspond to a standard 240 pin socket with one inside "KEY" contact, one outer "KEY" contact and four 'orientation' contacts plugged on the outside corner. The Pentium OverDrive processor itself (not the socket) **does not have** any "KEY" pins. The five contacts plugged on the outside corner ensure proper orientation for the Pentium OverDrive processor. The Pentium OverDrive processor pinout is shown in Figures 2-1 and 2-2.

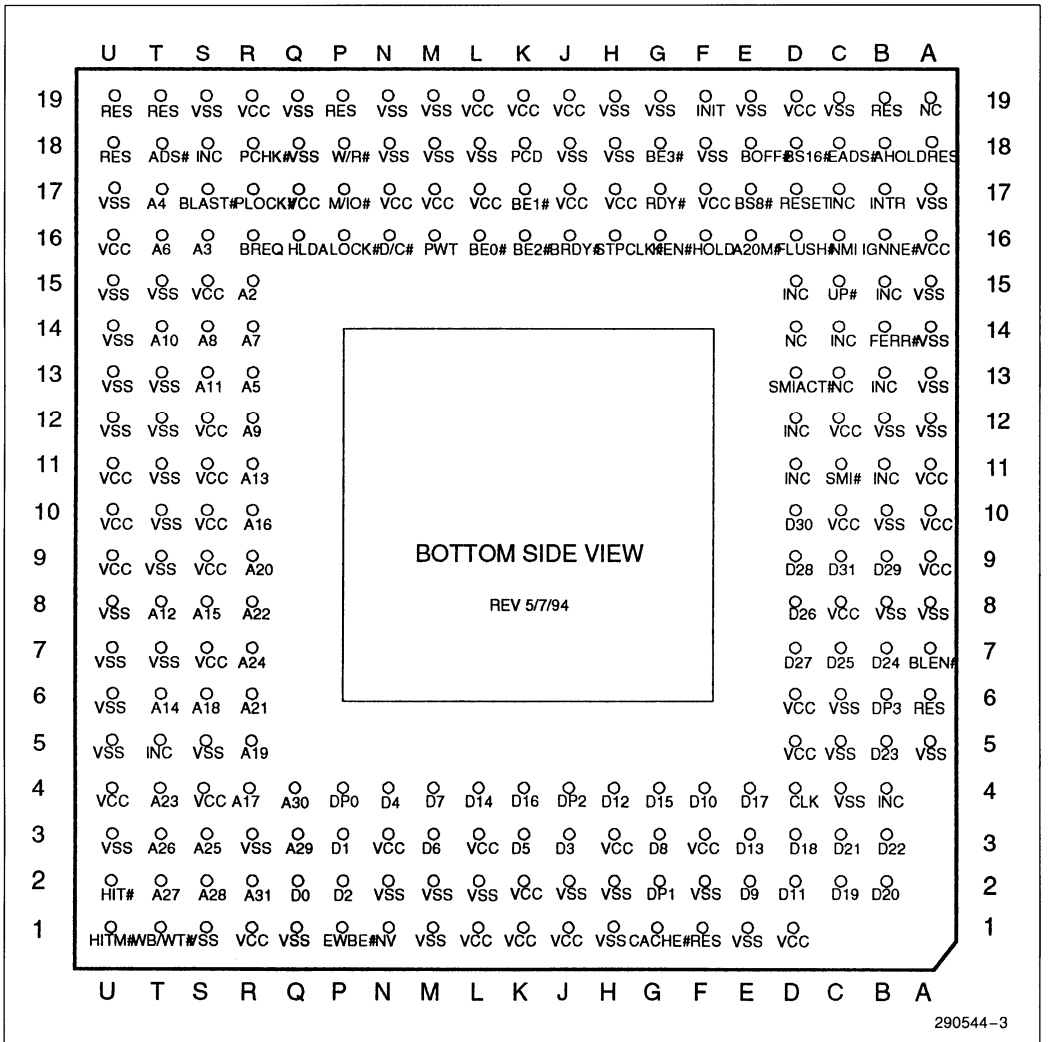
Please note that the boundary scan pins (**TCK, TDO,TDI,** and **TMS**), and all testability pins have been removed from the production version of the Pentium OverDrive processor. An engineering sample will be available that will allow the use of boundary scan and testability functions. For more information on boundary scan and testability pins, please contact Intel.

2.1 Pentium® OverDrive® Processor Pinout



***NOTE:**
Pin A1 is located in the lower left corner to make the labels on the top plate of Intel processors orient right side up. All "RES" and "NC" pins should be left unconnected to insure proper operation.

Figure 2-1. Pentium® OverDrive® Processor Pinout (Top Side View)



***NOTE:**
Pin A1 is located in the lower left corner to make the labels on the top plate of Intel processors orient right side up. All "RES" and "NC" pins should be left unconnected to insure proper operation.

Figure 2-2. Pentium® OverDrive® Processor Pinout (Bottom Side View)

2.2 Pin Cross Reference

Table 2-1. Pentium® OverDrive® Processor Pin Cross Reference

Address		Data		Control				N/C	V_{CC}		V_{SS}	
A2	R15	D0	Q2	A20M#	E16	INV	N1	A19		L1	A5	M18
A3	S16	D1	P3	ADS#	T18	KEN#	G16	D14	A9	L3	A8	M19
A4	T17	D2	P2	AHOLD	B18	LOCK#	P16		A10	L17	A12	N2
A5	R13	D3	J3	BE0#	L16	M/IO#	P17	**INC**	A11	L19	A13	N18
A6	T16	D4	N4	BE1#	K17	NMI	C16		A16	M17	A14	N19
A7	R14	D5	K3	BE2#	K16	PCD	K18	B11	C8	N3	A15	Q1
A8	S14	D6	M3	BE3#	G18	PCHK#	R18	B13	C10	N17	A17	Q18
A9	R12	D7	M4	BLAST#	S17	PLOCK#	R17	B4	C12	Q17	B8	Q19
A10	T14	D8	G3	BLEN#	A7	PWT	M16	B15	D1	R1	B10	R3
A11	S13	D9	E2	BOFF#	E18	RDY#	G17	C17	D5	R19	B12	S1
A12	T8	D10	F4	BRDY#	J16	RESET	D17	C13	D6	S4	C4	S5
A13	R11	D11	D2	BREQ	R16	SMI#	C11	C14	D19	S7	C5	S19
A14	T6	D12	H4	BS8#	E17	SMIACT#	D13	D11	F3	S9	C6	T7
A15	S8	D13	E3	BS16#	D18	STPCLK#	H16	D12	F17	S10	C19	T9
A16	R10	D14	L4	CACHE#	G1	UP#	C15	D15	H3	S11	E1	T10
A17	R4	D15	G4	CLK	D4	W/R#	P18	S18	H17	S12	E19	T11
A18	S6	D16	K4	D/C#	N16	WB/WT#	T1	T5	J1	S15	F2	T12
A19	R5	D17	E4	DP0	P4				J17	U4	F18	T13
A20	R9	D18	D3	DP1	G2				J19	U9	G19	T15
A21	R6	D19	C2	DP2	J4				K1	U10	H1	U3
A22	R8	D20	B2	DP3	B6			**RES**	K2*	U11	H2	U5
A23	T4	D21	C3	EADS#	C18				K19	U16	H18	U6
A24	R7	D22	B3	EWBE#	P1			A6			H19	U7
A25	S3	D23	B5	FERR#	B14			A18			J2	U8
A26	T3	D24	B7	FLUSH#	D16			B19			J18	U12
A27	T2	D25	C7	HIT#	U2			F1			L2	U13
A28	S2	D26	D8	HITM#	U1			P19			L18	U14
A29	Q3	D27	D7	HLDA	Q16			T19			M1	U15
A30	Q4	D28	D9	HOLD	F16			U18			M2	U17
A31	R2	D29	B9	IGNNE#	B16			U19				
		D30	D10	INIT	F19							
		D31	C9	INTR	B17							

*If designing for single socket compatibility with future Pentium OverDrive processors, pin K2 may be connected to V_{CC} via a circuit to limit the current through the pin. Please contact Intel for more information about compatibility with future Pentium OverDrive processors.

2.3 Pentium® OverDrive® Processor Pin Descriptions

This section provides a summary of the Pentium OverDrive processor pins and how they function. For more information on the pinout differences between the Write-Back Enhanced IntelDX2 processor and the Pentium OverDrive processor, please see Section 10.

2.3.1 SIGNAL DESCRIPTIONS

Table 2-2 provides a brief pin description.

Table 2-2. Signal Description

Symbol	Type	Name and Function
INTERRUPTS		
INIT	I	The **INIT** pin is the Pentium OverDrive processor initialization pin. Since the SL-enhanced Intel486 processors implement this functionality on the **SRESET** pin, the corresponding pin (D11) on the Pentium OverDrive Processor is defined as an **INC** pin so that pin F19 and pin D11 may be tied together on the motherboard. **INIT** will force the Pentium OverDrive Processor to begin execution in a known state. The processor state after **INIT** is the same as the state after **RESET** except that the internal caches, floating point registers, and the SMM base register retain whatever values they had prior to **INIT. INIT** may NOT be used in lieu of **RESET** after power-up. **INIT** can not be used to cause the processor to enter BIST or Tri-State Test Mode. INIT is an edge triggered interrupt and is processed at instruction boundaries. Since **INIT** is an interrupt, **ADS#** may be driven even if **INIT** is active. Recognition of **INIT** is guaranteed in a specific clock if it is asserted synchronously and meets setup and hold times. To guarantee recognition if **INIT** is asserted asynchronously, it must have been deasserted for a minimum of two clocks before being returned active to the processor and remain asserted for a minimum pulse width of two clocks. **INIT** must remain active for three clocks prior to the **BRDY#** or **RDY#** of I/O write cycle to guarantee the processor recognizes and performs **INIT** right after I/O write instruction. **INIT** is asynchronous but must meet setup and hold times t_{20} and t_{21} to be recognized on any one clock. **INIT** is supplied with an internal pull-down.
CACHE CONTROL		
WB/WT#	I	This pin allows a cache line to be defined as *write back or write through* on a line by line basis. As a result, it controls the MESI state that the line is saved in. This pin is sampled in the clock in which the first **BRDY#** or **RDY#** is returned for a read cycle or a write through cycle. However, it must the meet setup and hold times at every clock. Cache lines are not allocated on write through cycles. This pin is also used as a configuration pin at the falling edge of **RESET** only. If **WB/WT#** is driven low, or left unconnected, the processor will operate in a **standard bus (write through only)** mode. This means that the Pentium OverDrive processor will run in an IntelDX2 processor compatible write through only cache mode. If **WB/WT#** is driven high, the processor will operate in enhanced bus **(write back)** mode. **INIT** can not be used to change the mode of the processor with **WB/WT#.** During **RESET, WB/WT#** should be held at its desired value for two clocks before and after the falling edge of **RESET. WB/WT#** is ignored when the processor is in **standard bus** mode. Please see Section 3 for a detailed description of the two modes of operation. **WB/WT#** has an internal pull down resistor to force the processor into the **standard bus** mode if left unconnected. The pin timings must meet setup and hold times t_{38} and t_{39} on every clock edge.

Table 2-2. Signal Description (Continued)

Symbol	Type	Name and Function
CACHE INQUIRE		
EWBE#	I	The *External Write Buffer Empty* pin, when inactive (HIGH), indicates that a write through cycle is pending in the external system. When the processor generates a non-write back cycle, and **EWBE#** is sampled inactive, the processor will hold off all subsequent writes to all E- or M- state lines until all write-through cycles have completed, as indicated by **EWBE#** going active. This ensures that writes are visible from outside the processor in the same order as they were generated by software. When the Pentium OverDrive processor serializes instruction execution through the use of a serializing instruction, it waits for **EWBE#** to go active before fetching and executing the next instruction. **EWBE#** is sampled with each **BRDY#** or **RDY#** of a write through cycle. If sampled inactive, the processor will repeatedly sample **EWBE#** in each clock until it is found active. Once sampled active, it will ignore **EWBE#** until the next **BRDY#** or **RDY#** of a write cycle. **EWBE#** is not sampled and has no effect on processor operation while the processor is in standard bus mode. If unused, **EWBE#** should be tied LOW or left unconnected. **EWBE#** is active low and must meet setup and hold times t_{38} and t_{39} and is supplied with an internal pull-down.
HIT#	O	This pin participates in an inquire cycle. If an inquire cycle hits a valid line in the processor, this pin is asserted two clocks after **EADS#** has been driven to the processor. If the inquire cycle misses in the processor cache, this pin is negated two clocks after **EADS#**. This pin changes its value only as a result of inquire cycle as described above and retains its value between any two inquire cycles.
HITM#	O	**HITM#** is asserted when an inquire cycle hits a modified line in the Pentium OverDrive processor. It can be used to inhibit another bus master from accessing the data until the line is completely written back. **HITM#** is asserted two clocks after an **EADS#** assertion hits a modified line in the processor cache and deasserts after the last **BRDY#** or **RDY#** of the corresponding write back is returned. **HITM#** is guaranteed to be deasserted before the **ADS#** following a write back cycle. If an INVD instruction occurs at the same time as an external snoop, **HITM#** may be asserted and deasserted without a corresponding **ADS#** for a write back cycle.
CACHE BURST CONTROL		
BLEN#	I	**BLEN#** controls if write back cycles will be attempted to run as burst cycles. When **BLEN#** is HIGH, the processor will write out a dirty line as four separate writes, each with its own **ADS#** and **BLAST#**. When **BLEN#** is LOW, a write back is done as a 16 byte burst. Since **BLEN#** is a constant input, meaning that it will have to be tied HIGH or LOW. As a result, it does not have setup and hold time specifications. **BLEN#** is has no effect and is not sampled when the processor is in **standard bus** mode. **BLEN#** is supplied with an internal pull-up resistor.
CACHE#	O	The **CACHE#** pin is used to indicate a cache operation. **CACHE#** will be active along with the first **ADS#** until the first **RDY#/BRDY#** and is undefined during any other time period. On cacheable read accesses, **CACHE#** will be asserted when **PCD** is low, except on locked cycles. **CACHE#** will always be asserted in the beginning of cacheable reads (line fills and code prefetches) and can be used as an indication that the processor intends to perform a linefill. For write cycles, **CACHE#** is active for write backs only. The beginning of a replacement write back can be uniquely identified by the presence of **ADS#, W/R#** and **CACHE#** together. The beginning of a snoop write back is marked by **ADS#, W/R#, CACHE#** and **HITM#** being active together.

Table 2-2. Signal Description (Continued)

Symbol	Type	Name and Function
OEM CPU INTERFACE		
UP#	O	The *upgrade present* pin is used to signal the system OEM microprocessor to float its outputs and stop driving the bus. It is active low and is never floated. **UP#** is driven low at power-up and remains active for the entire duration of the Pentium OverDrive processor operation.
INC PINS		
INC		The **INC** pin is defined to be an *internal no-connect*. This means that the pin is not connected internally, and may be used for the routing of external signals. It will never be used for any other function, and is guaranteed to remain an **INC** pin. Any voltage level applied to an **INC** pin must remain within the processor V_{CC} specifications. Most **INC** pins have a specified use in creating a design that supports multiple processors in one socket. For more information, please see Section 9.

2.3.2 OUTPUT PINS

Table 2-3 lists all the output pins, indicating their active level, and when they are floated.

Table 2-3. Output Pins

Name	Active Level	When Floated
BREQ	HIGH	
HLDA	HIGH	
BE3#–BE0#	LOW	Bus Hold, Backoff
PWT, PCD	HIGH	Bus Hold, Backoff
W/R#, D/C#, M/IO#	LOW	Bus Hold, Backoff
LOCK#	LOW	Bus Hold, Backoff
PLOCK#	LOW	Bus Hold, Backoff
ADS#	LOW	Bus Hold, Backoff
BLAST#	LOW	Bus Hold, Backoff
PCHK#	LOW	
FERR#	LOW	
SMIACT#	LOW	
A3–A2	HIGH	Bus Hold, Address Hold and Backoff
HIT#, HITM#	LOW	
CACHE#	LOW	Bus Hold, Backoff
UP#	LOW	

2.3.3 INPUT PINS

Table 2-4 lists all input pins, indicating their active level, and whether they are synchronous or asynchronous inputs.

Table 2-4. Input Pins

Name	Active Level	Synchronous/ Asynchronous	Internal Resistor	Qualified
CLK				
RESET	HIGH	Asynchronous		
HOLD	HIGH	Synchronous		
AHOLD	HIGH	Synchronous	PULLDOWN	
EADS#	LOW	Synchronous	PULLUP	
BOFF#	LOW	Synchronous	PULLUP	
FLUSH#	LOW	Asynchronous	PULLUP	
A20M#	LOW	Asynchronous	PULLUP	
BS16#, BS8#	LOW	Synchronous	PULLUP	
KEN#	LOW	Synchronous	PULLUP	
RDY#	LOW	Synchronous		
BRDY#	LOW	Synchronous	PULLUP	
INTR	HIGH	Asynchronous		
NMI	HIGH	Asynchronous		
IGNNE#	LOW	Asynchronous	PULLUP	
BLEN#	LOW	Tie High or Low	PULLUP	
EWBE#	LOW	Synchronous	PULLDOWN	BRDY#/RDY#
INIT	HIGH	Asynchronous	PULLDOWN	
INV	HIGH	Synchronous	PULLUP	EADS#
STPCLK#	LOW	Asynchronous	PULLUP	
SMI#	LOW	Asynchronous	PULLUP	
WB/WT#	BOTH	Synchronous	PULLDOWN	FIRST RDY#/RDY#

2.3.4 INPUT/OUTPUT PINS

Table 2-5 lists all the input/output pins, indicating their active level, and when they are floated.

Table 2-5. Input/Output Pins

Name	Active Level	When Floated
D31–D0	HIGH	Bus Hold, Backoff
DP3–DP0	HIGH	Bus Hold, Backoff
A31–A4	HIGH	Bus, Address Hold, Backoff

3.0 CACHE FUNCTIONALITY

3.1 Cache Introduction

Special hooks are provided to support the Pentium OverDrive processor on-chip write back cache and to maintain cache consistency. The external environment can dynamically change the caching policy of the Pentium OverDrive processor on a line by line basis.

The Pentium OverDrive processor has separate code and data caches. Each of the caches are 16 Kbytes in size and each is organized as a 4-way set associative cache. The data cache follows the MESI cache consistency protocol while the code cache follows a subset of that protocol. For a complete description of the cache see the *Intel486 Microprocessor Family Data Book*(2).

NOTE:

2. A generic discussion on the operation of cache memories can be found in the Intel Cache Tutorial available from your Intel sales representative or from Intel's Literature department, order #296543-002.

3.2 Cache Organization

The Pentium OverDrive processor includes separate code and data caches on chip to meet its performance goals. The code and data caches can be accessed simultaneously. The code cache can provide up to 16 bytes of raw opcodes and the data cache can provide data for two data references all in the same clock. Each of the caches are accessed with physical addresses and each cache has its own TLB (translation look aside buffer) to translate linear addresses to physical addresses. A cache consistency protocol called the **MESI** protocol is implemented in the data cache to ensure data consistency in a multiprocessor environment.

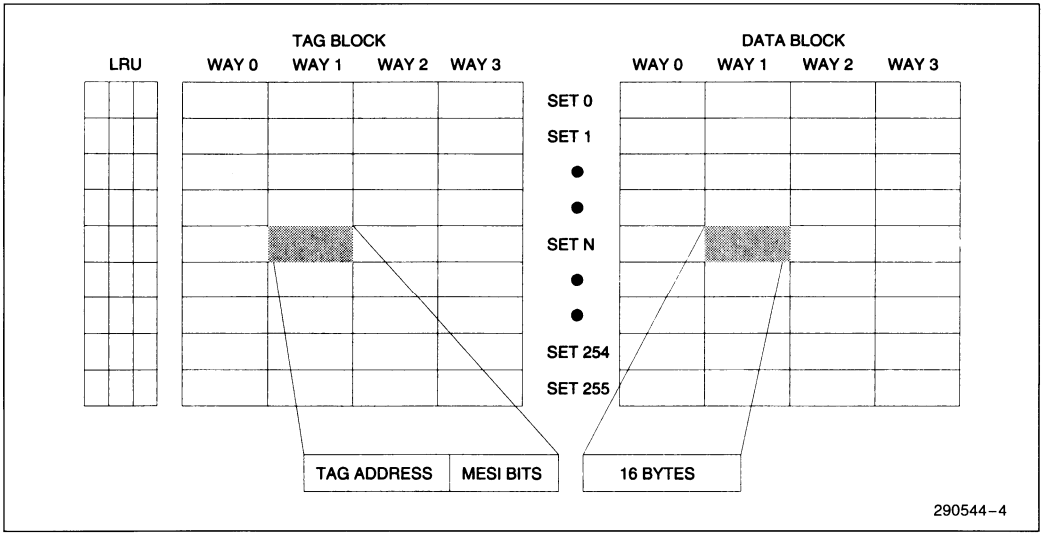


Figure 3-1. Conceptual Organization of Data Cache

Each of the caches are 16 Kbytes in size and each is organized as a 4-way set associative cache. There are 256 sets in each cache, each set containing 4 lines. Each cache line is 16 bytes wide. Replacement in both the data and instruction caches is handled by a pseudo LRU mechanism which requires three bits per set in each of the caches. A conceptual diagram of the organization of the data cache is shown below in Figure 3-1.

The data cache can support two data references simultaneously in one clock, one from each of the two pipelines. It is a write back cache with full support for data consistency in a multimaster environment. This is implemented with two status bits associated with each cache line. The data cache can optionally be configured in write through mode on a line by line basis when in write back cache mode. The storage array in the data cache is single ported but interleaved on 4 byte boundaries to be able to provide data for two simultaneous accesses to the same cache line. The tags in the data cache are triple ported. One of the ports is dedicated to snooping while the other two are used to lookup two independent addresses corresponding to data references from each of the pipelines. The code cache tags are also triple ported. Again, one port is dedicated to support snooping and other two ports facilitate split line accesses (simultaneously accessing upper half of one line and lower half of the next line).

The data cache has a 4-way set associative, 64-entry TLB for 4 KB pages and a separate 4-way set associative, 8-entry TLB to support 4 MB pages. The code cache has one 4-way set associative, 32-entry TLB for 4 KB pages as well as 4 MB pages which are cached in 4 KB increments. The TLBs associated with the instruction cache are single ported whereas the data cache TLBs are fully dual ported to be able to translate two independent linear addresses for two data references simultaneously. Replacement in the TLBs is handled by a pseudo LRU mechanism (similar to the Intel486™ CPU) that requires 3 bits per set. The tag and data arrays of the TLBs are parity protected with a parity bit associated with each of the tag and data entries in the TLBs.

3.3 State Transition Tables

Lines cached in the Pentium OverDrive processor can change state because of Pentium OverDrive processor generated activity or as a result of activity on the Pentium OverDrive processor bus generated by other bus masters (snooping). As shown in the following tables, state transitions occur because of Pentium OverDrive processor generated transactions (memory reads/writes) and snooping by the external system. This protocol has minor differences from the MES1 protocol of the Write-Back Enhanced IntelDX2 processor as detailed in Section 10.2.

3.3.1 READ CYCLE

The state transitions for the data cache during reads are shown in Table 3-1. For a cache line that is in the M (Modified), E (Exclusive) or S (Shared) states, the data is transferred from the cache to the core, with no bus cycle generated.

Three different cases can occur when a cache read occurs for an I-state (Invalid) line. An access to an invalid line indicates a miss in the cache, so a read cycle will be generated. If the **CACHE#** and **KEN#** pins are sampled low, and **WB/WT#** is high, then the line will be stored in the E-state in the cache. **WB/WT#** is sampled with the first **BRDY#** or **RDY#** of the transfer, while **KEN#** is sampled one clock before the first **RDY#** or **BRDY#.** If the **CACHE#** and **KEN#** are low, and **WB/WT#** is low, then the cache will be defined as write-through. If **PWT** is HIGH, cache line fills will always be stored as shared lines, even if **WB/WT#** is high. This will cause the line to be stored in a S state. If either **CACHE#** or **KEN#** is high, then the line is non-cacheable, so it will remain in the I state.

Table 3-1. Data Cache State Transitions for Pentium® OverDrive® Processor Initiated Unlocked Read Cycles

Present State	Pin Activity	Next State	Description
M	n/a	M	Read hit; data is provided to the Pentium OverDrive processor core by cache. No bus cycle is generated.
E	n/a	E	Read hit; data is provided to the Pentium OverDrive processor core by cache. No bus cycle is generated.
S	n/a	S	Read hit; Data is provided to the Pentium OverDrive processor by the cache. No bus cycle is generated.
I	**CACHE#** low AND **KEN#** low AND **WB/WT#** high AND **PWT** low	E	Data item does not exist in cache (MISS). A bus cycle (read) will be generated by the Pentium OverDrive processor. This state transition will happen if **WB/WT#** is sampled high with first **BRDY#** or **RDY#**.
I	**CACHE#** low AND **KEN#** low AND (**WB/WT#** low OR **PWT** high)	S	Same as previous read miss case except that **WB/WT#** is sampled low with first **BRDY#** or **RDY#**. If **PWT** is high, **WB/WT#** is ignored and the resulting line state is always "S".
I	**CACHE#** high OR **KEN#** high	I	**KEN#** pin inactive; the line is not intended to be cached in the Pentium OverDrive processor.

NOTE:
The transition from I to E or S-states (based on **WB/WT#**) happens only if the line is cacheable. If **KEN#** is sampled high, the line is not cached and remains in the I-state.

3.3.2 WRITE CYCLE

The state transitions of data cache lines during Pentium OverDrive processor generated write cycles are illustrated in Table 3-2. Writes to SHARED lines in the data cache are always sent out on the bus along with updating the cache with the write item. The status of the **PWT** and **WB/WT#** pins during these write cycles on the bus determines the state transitions in the data cache during writes to S-state lines.

A write to a SHARED line in the data cache will generate a write cycle on the Pentium OverDrive processor bus to update memory and/or invalidate the contents of other caches. If the **PWT** pin is driven high when the write cycle is run on the bus, the line will be updated, and will stay in the S- state regardless of the status of the **WB/WT#** pin that is sampled with the first **BRDY#** or **RDY#**. If **PWT** is driven low, the status of the **WB/WT#** pin sampled along with the first **BRDY#** or **RDY#** for the write cycle determines what state (E or S) the line transitions to.

The state transition from S to E is the only transition in which the data and the status bits are not updated at the same time. The data will be updated when the cycle is written to the Pentium OverDrive processor write buffers. The state transition does not occur until the write has completed on the bus (last **BRDY#** or **RDY#** has been returned). Writes to the line after the transition to the E-state will not generate bus cycles. However, it is possible that writes to the same line that were buffered before the transition to the E-state will generate bus cycles after the transition to E-state.

An inactive **EWBE#** input will stall subsequent writes to an E- or an M- state line until **EWBE#** is returned active.

Table 3-2. Data Cache State Transitions for Pentium® OverDrive® Processor Initiated Write Cycles

Present State	Pin Activity	Next State	Description
M	n/a	M	Write hit; update data cache. No bus cycle generated to update memory.
E	n/a	M	Write hit; update cache only. No bus cycle generated; line is now MODIFIED.
S	**PWT** low AND **WB/WT#** high	E	Write hit; data cache updated with write data item. A write through cycle is generated on bus to update memory and/or invalidate contents of other caches. All subsequent writes to E- or M-state lines are held off until completion of write cycle is known and state transition happens.
S	**PWT** low AND **WB/WT#** low	S	Same as above case of write to S-state line except that **WB/WT#** is sampled low.
S	**PWT** high	S	Same as above cases of writes to S-state lines except that this is a write hit to a line in a write-through page; status of **WB/WT#** pin is ignored.
I	n/a	I	Write MISS; a write through cycle is generated on the bus to update external memory. No allocation is done.

NOTE:
Memory writes are buffered while I/O writes are not. There is no guarantee of synchronization between completion of memory writes on the bus and instruction execution after the write.

3.3.3 INQUIRE CYCLES (SNOOPING)

The purpose of inquire cycles is to check whether the address being presented is contained within the caches in the Pentium OverDrive processor. Inquire cycles may be initiated with or without an invalidation request (**INV** = 1 or 0). The processor samples the snoop address during the clock that **EADS#** is active. An inquire cycle is run through the data and code caches through a dedicated snoop port to determine if the address is contained in one of the Pentium OverDrive processor caches. If the address is in a Pentium OverDrive processor cache, the **HIT#** pin is asserted. If the address hits a modified line in the processor , the **HITM#** pin is also asserted and the modified line is then written back to external memory.

Table 3-3 shows the state transitions for inquire cycles.

3.4 Processor Code Cache Consistency Protocol

The Pentium OverDrive processor code cache follows a subset of the MESI protocol. Access to lines in the code cache are either a Hit (Shared) or a Miss (Invalid). In the case of a read hit, the cycle is serviced internally to the Pentium OverDrive processor and no bus activity is generated. In the case of a read miss, the read is sent to the external bus and may be converted to a line fill.

Lines are never overwritten in the code cache. Writes generated by the Pentium OverDrive processor are snooped by the code cache. If there is a hit, the line is invalidated. If there is a miss, no action is taken by the code cache.

3.5 Warm Reset Cache Behavior

The **INIT** pin can be used to reset the Pentium OverDrive processor without invalidating the on-chip cache. The Pentium OverDrive processor state after **INIT** is the same as the state after **RESET** except that the internal caches, floating point registers, and SMM Base Register retain whatever values they had prior to recognition of **INIT**. The **INIT** signal can be used instead of **RESET** for warm resets when the cache contents need to be maintained. However, **INIT** cannot be used in lieu of **RESET** after power up. For more information on the INIT and the Pentium OverDrive processor, please see Section 5.

Table 3-3. Cache State Transitions during Inquire Cycles

Present State	Next State INV = 1	Next State INV = 0	Description
M	I	S	Snoop hit to a MODIFIED line indicated by **HIT#** and **HITM#** pins low. Pentium OverDrive processor schedules the writing back of the modified line to memory.
E	I	S	Snoop hit indicated by **HIT#** pin low; no bus cycle generated.
S	I	S	Snoop hit indicated by **HIT#** pin low; no bus cycle generated.
I	I	I	Address not in cache; **HIT#** pin high.

4.0 HARDWARE DESIGN CONSIDERATIONS

4.1 Introduction

This section describes the organization of the Translation Lookaside Buffers (TLBs), write buffers and the buffering scheme used in the Pentium OverDrive processor. Other important Pentium OverDrive Processor design specific details are also included as well as the use of the **WB/WT#** pin as an input to determine the fundamental cache operation mode of the processor.

4.1.1 CACHE CONSISTENCY CYCLES

The external system can check and invalidate cache lines in the internal processor cache using inquire cycles (snooping). Snooping allows the external system to keep cache coherency throughout the system. Snoop cycles may be performed using **AHOLD, BOFF#,** or **HLDA** and then asserting **EADS#** to inform the processor that the snoop address is available on the bus. The following table summarizes the snoop mechanism initiated by any of these three control signals.

The snoop cycle begins by checking whether a particular cache line has been "cached" and invalidates the line based on the state of the **INV** pin. If the Pentium OverDrive processor is configured in the Standard Bus Mode, the processor will always invalidate the cache line on snoop hits. If the processor is configured in the Enhanced Bus Mode, the system must drive **INV** high to invalidate a particular cache line. The Pentium OverDrive processor will invalidate the line and write back an E-state line if the system snoop hits either S-state, E-state, or M-state line, provided **INV** was driven high during **EADS#** assertion. If **INV** is driven low, a modified line will be written back to memory and will remain in the cache as a write-back line. If **INV** is driven low, a shared line also will continue to remain in the cache as a shared line.

After asserting **AHOLD** or **BOFF#,** the external master driving a snoop cycle must wait at least two clocks before asserting **EADS#.** If snooping is done after **HLDA** assertion, then the master performing a snoop must wait for at least one clock cycle before driving the snoop addresses and asserting **EADS#. INV** should be driven low during bus master read operations to minimize invalidations. **INV** should be driven high to invalidate a cache line during bus master write operations. The Pentium OverDrive processor asserts **HIT#** and **HITM#** if the cycle hits an M state line in the cache or **HIT#** only if the cycle

Table 4-1. Snoop Cycles under AHOLD, BOFF#, or HLDA

AHOLD	Tri-states the address bus. **ADS#** will be asserted under **AHOLD** only to initiate a snoop writeback cycle. An ongoing burst cycle will complete under an **AHOLD.** For non-burst cycles, a specific non-burst transfer (**ADS#-RDY#** transfer) will complete under **AHOLD** and will be fractured (interrupted) before the next assertion of **ADS#.** A snoop writeback cycle will be reordered ahead of a fractured non-burst cycle. Should an **ADS#** be required to start the next cycle while **AHOLD** is asserted, the processor will only perform snoop write back cycles. If the processor issues and **ADS#** while **AHOLD** is asserted, it is the responsibility of the system to determine the address of the snoop write back from the snoop address driven with **EADS#.** An interrupted non-burst cycle will be completed only after the snoop writeback cycle is completed, provided there are no other snoop writeback cycles scheduled and **AHOLD** is deasserted. If **BLEN#** is driven inactive (disabling bursted writes), the processor will drive four individual **ADS#-RDY#** cycles to complete the cycle while **AHOLD** is active.
BOFF#	Overrides **AHOLD;** takes effect in the next clock. Ongoing bus cycles will stop in the clock following **BOFF#** being asserted and resumes when **BOFF#** is deasserted, in the same manner as the standard Intel486 processor bus. A snoop writeback will be reordered ahead of the backed off cycle. The snoop writeback cycle begins after **BOFF#** is deasserted followed by any backed off cycle.
HOLD	**HOLD** will be acknowledged only between bus cycles, except for a non-cacheable, non-bursted code prefetch cycle. In a non-cacheable, non-bursted code prefetch cycle, **HOLD** is acknowledged after the system returns **RDY#** or if **BOFF#** is asserted. Once **HLDA** is active, the processor blocks all bus activities until the system releases the bus (by de-asserting **HOLD**).

hits an E or S state line. These output signals become valid two clock periods after **EADS#** is valid on the bus. **HITM#** will remain asserted at least until the last **RDY#** or **BRDY#** of the snoop writeback cycle is returned. The **HIT#** signal will continue to drive the result of the last snoop until the next external snoop occurs. Most timing diagrams in the following sections do not include the **HIT#** signal since it is not necessary for single processor system designs. Snoop operations may interrupt an ongoing bus operation in both the Standard Bus Mode and Enhanced Bus Mode.

The Pentium OverDrive processor can accept EADS# in every clock period while in the Standard Bus Mode. In the Enhanced Bus Mode, the processor can accept EADS# every other clock period until the external snoop hits an M-state line. Any **EADS#** assertion after the **EADS#** that hit a modified line will be ignored. The processor will not accept any further **EADS#** assertions until the snoop writeback operation is completed and **HITM#** is deasserted. Figure 4-1 shows the allowable **EADS#** window for the different snooping mechanisms (**AHOLD, HOLD, BOFF#**). **For the Enhanced bus mode, EADS# must not be asserted outside the windows presented in the diagrams below.**

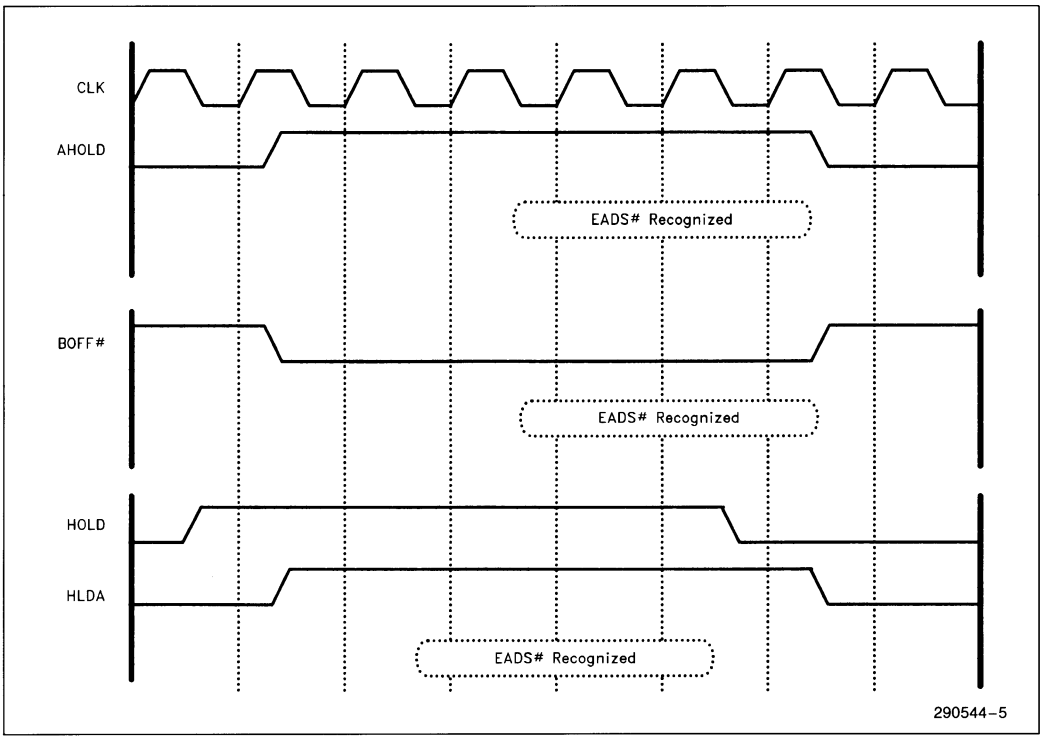


Figure 4-1. EADS# Snooping Window

Figure 4-2 shows that the processor can accept an **EADS#** assertion only every other clock while in enhanced bus mode.

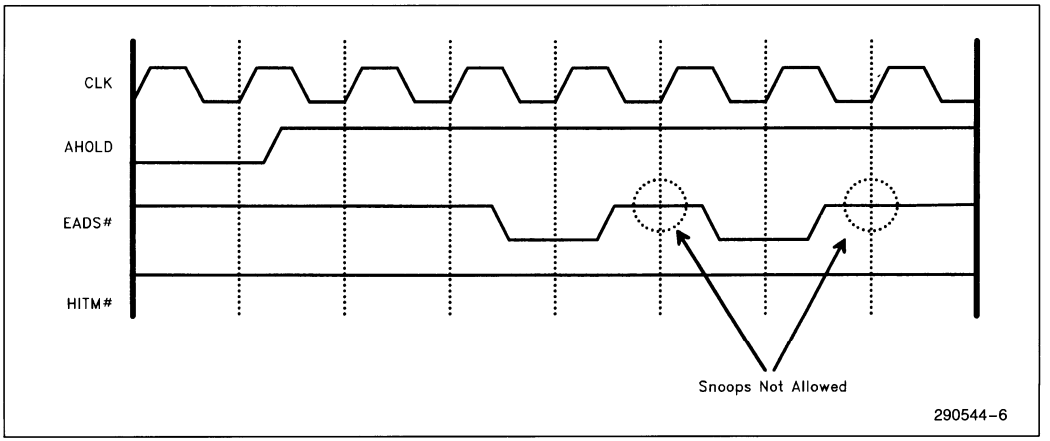


Figure 4-2. EADS# Snooping Frequency in Enhanced Bus Mode

4.1.2 WRITE BACK CYCLES

Writeback cycles may be bursted or non-bursted by returning **RDY#** or **BRDY#**. All writeback operations write 16 bytes of data to memory corresponding to the modified line in the cache. **BS8# and BS16# are not allowed during writeback cycles.**

The state of **BLEN#** determines how a 16 byte line is written back. When **BLEN#** is LOW, the write back is done as a 16-byte burst transfer. **BRDY#** or **RDY#** may terminate each transfer. At the fourth transfer, **BLAST#** will signify the end of the write back. A write back when **BLEN#** is LOW but **RDY#** is used rather than **BRDY#** is shown in Figure 4-4. When **BLEN#** is HIGH, the 16-byte write back will be done as four consecutive 4 byte writes, each with its own **ADS#** and **BLAST#**. (See Figure 4-5).

BLEN# is not a dynamic pin since it cannot be toggled on a cycle per cycle basis. It cannot be changed once power has been applied to the system, so it should be tied HIGH or LOW.

The **CACHE#** pin is used to indicate that a cache operation is taking place. **CACHE#** is active with the first **ADS#** for both write backs and line fills, and is terminated by the first **RDY#/BRDY#**. An occurrence of **ADS#** = 0, **W/R#** = 1, and **CACHE#** = 0 indicates that a replacement write back is starting. The occurrence of **HITM#** = 0 during the above operation signifies that a snoop write back is occurring. Write back cycles begin at address 0x0 of the 16-byte line being pushed out. The burst order is the standard Intel486 Processor order of 0x0, 0x4, 0x8 and 0xC. If the write back is done as four separate writes, then each write will push out four bytes starting at byte 0x0. **PCD** and **CACHE#** are low during write back cycles, while **KEN#** is ignored.

BS8#, BS16# are ignored during write back cycles. After the last **BRDY#/RDY#** of a write back cycle is asserted, the Pentium OverDrive Processor will wait at least one **CLK** before issuing the next **ADS#**. In other words, a dead clock is inserted by the processor after the last transfer in a write back cycle. The dead clock is between the last **BRDY#/RDY#**, and the next **ADS#**. The dead clock appears only after the write back is complete, so there are no dead clocks between individual transfers of a write back. This dead clock time is used by the Pentium OverDrive processor to complete internal cache operations.

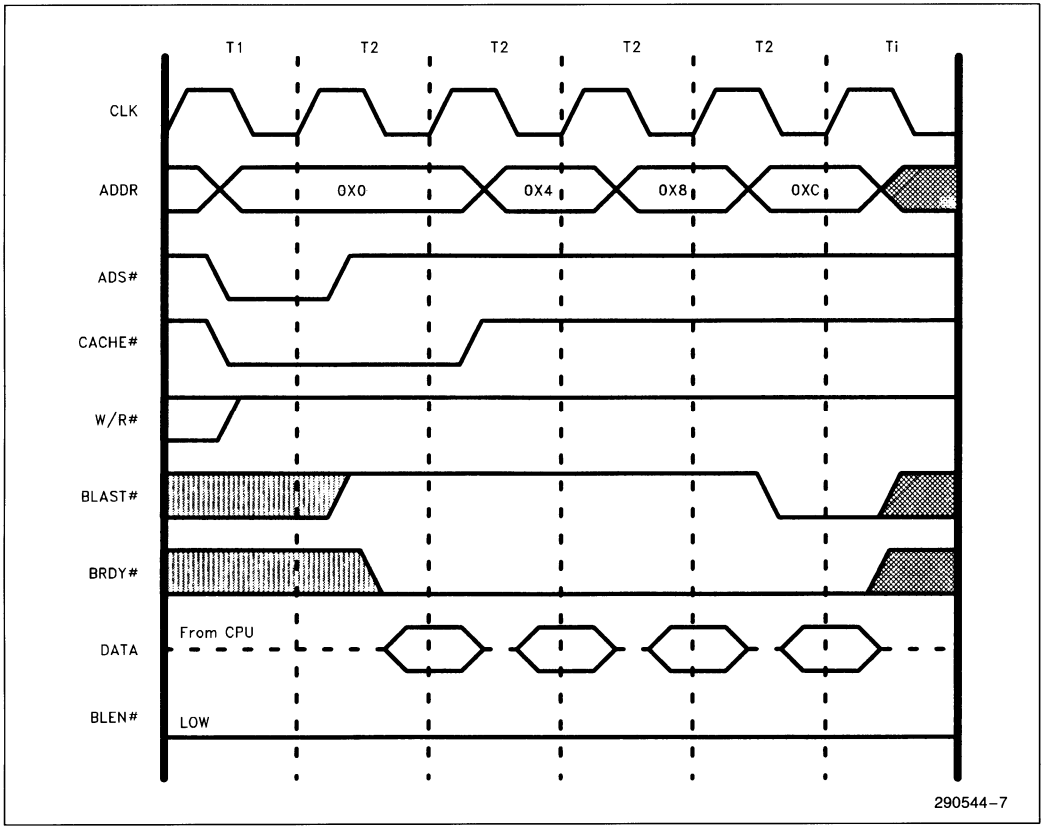


Figure 4-3. Write Back Operation—BLEN# Active

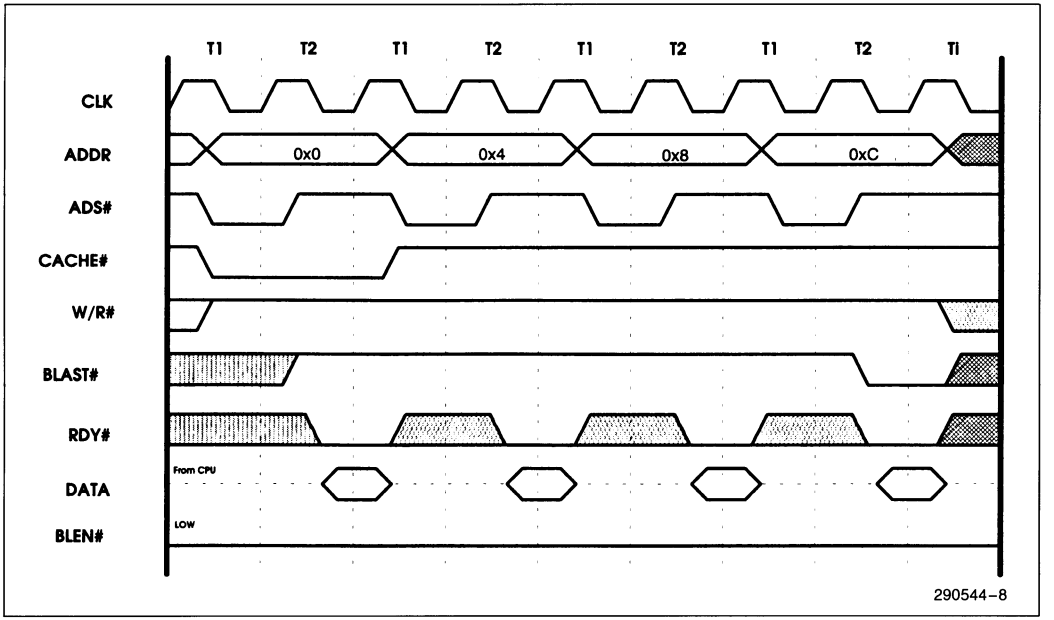


Figure 4-4. Write Back with BLEN# Active Using RDY#

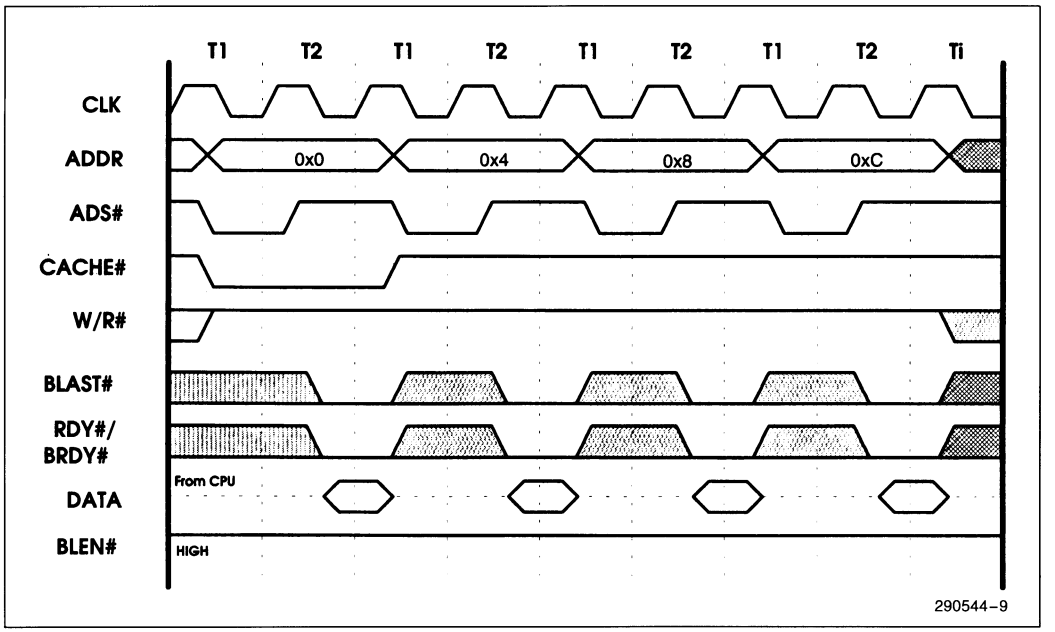


Figure 4-5. Write Back as Four 4-Byte Transfers (BLEN# Inactive)

4.2 WB/WT# As an Initialization Input

To make the Pentium OverDrive processor more compatible with the IntelDX2 processor, several small enhancements have been added to the processor to help distinguish different processor modes of operation. These two modes will be referred to as **"standard bus mode" (Write through processor cache only)** and "enhanced bus mode" (Write back processor enabled and are discussed in the following paragraphs.

In order to allow the Pentium OverDrive processor to operate in more of an IntelDX2 processor manner, the **WB/WT#** pin is used as an initialization input to configure the operating mode of the processor. At the falling edge of **RESET,** the processor can be configured to operate in a write through only (IntelDX2 CPU compatible) L1 cache mode (**standard bus** mode), or in a write back L1 cache mode (enhanced bus mode). Once a mode is selected, the processor will continue to operate in the selected mode and can only be changed to a different mode by starting the **RESET** process again. Assertion of **INIT** will not change the operating mode of the processor. **WB/WT#** has an internal pulldown that will force any design that leaves **WB/WT#** unconnected into the write through mode of operation. Table 4-2 lists the two modes of operation and the differences between them.

For more information on the effect of the mode operation on the various signals mentioned above, please see the *Intel486 Microprocessor Family Data Book*. Unless otherwise mentioned, all other functions of the Pentium OverDrive processor remain identical in both operating modes.

4.3 INIT Functionality

INIT behaves like an edge triggered interrupt on the Pentium OverDrive processor while in both enhanced bus mode (**WB/WT#** = HIGH at **RESET**) and standard bus mode (**WB/WT#** = LOW at **RESET**). Therefore, when **INIT** is asserted, there is a high probability that one or more bus cycles will be run by the processor while **INIT** is HIGH. The following figures demonstrate two scenarios of how the processor can issue an **ADS#** while **INIT** is asserted. Although the figures assume that an initial I/O write causes the **INIT** to be asserted by the support logic, these cases apply whenever **INIT** is HIGH. The first figure describes cycles being run by the processor before **INIT** is recognized. The second details cycles being run after **INIT** has been recognized.

Figure 4-6 shows the **INIT** signal being triggered by an I/O write. Even though **INIT** is asserted immediately, there is a pending prefetch which executes before the **INIT** is recognized.

Table 4-2. Effects of WB/WT# Initialization

State of WB/WT# at Reset Falling	Affect on Processor Operation
WB/WT# = LOW	Processor is in **Standard Bus** Mode ** IntelDX2 Processor Compatible ** 1: No Special **FLUSH#** Acknowledge Cycles are run on the bus after the assertion of the FLUSH# pin. 2: When **FLUSH#** is asserted, the caches will be invalidated in 15–20 system **CLKs**. 3: All Write Back specific inputs are ignored—(**BLEN#, EWBE#, WB/WT#, INV**) 4: **EADS#** is sampled at any time.
WB/WT# = HIGH	Processor is in **Enhanced Bus** Mode ** Intel486 Processor Write Back Bus Operation ** 1: The special **FLUSH#** Acknowledge Cycles will be run on the bus after the assertion of the **FLUSH#** and all the cache write backs (if any) are complete. 2: Write backs will be performed if a cache flush is requested (i.e.: **FLUSH#, WBINVD** inst . . .). The flush will take about 2000+ clocks. The system must watch for the FLUSH# special cycles to determine the end of the flush. 3: **WB/WT#** is sampled on a line by line basis to determine the storage state of a cache line on reads and writes. 4: The **BLEN#, EWBE#** and **INV** are no longer ignored. 5: **EADS#** is sampled only when the processor is an a **HOLD, AHOLD,** or **BOFF#** state. 6: **PLOCK#** is inactive and driven HIGH.

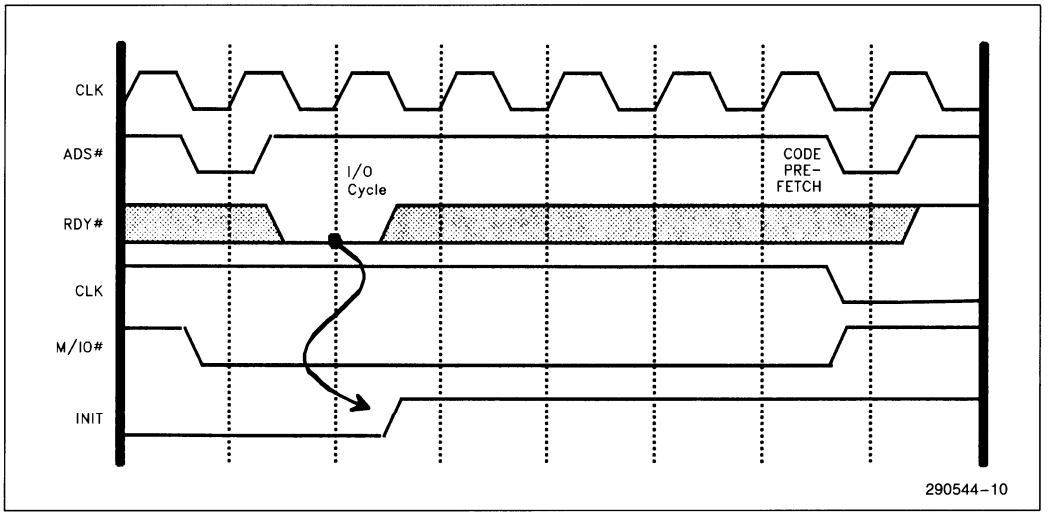


Figure 4-6. ADS# Issued during INIT: Case 1

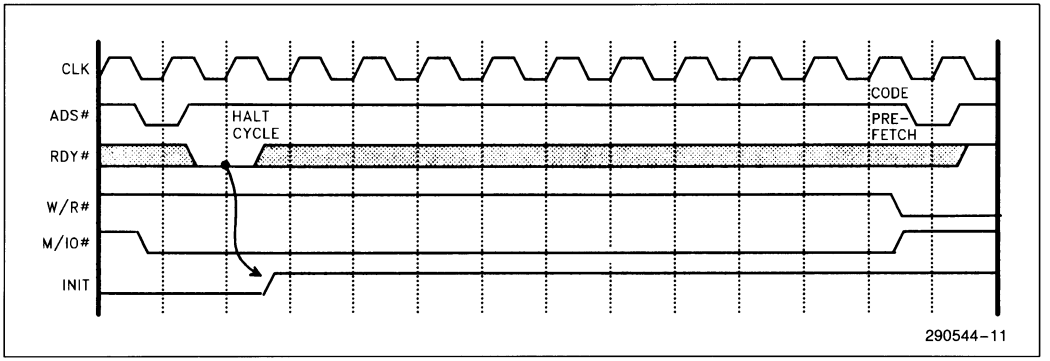


Figure 4-7. ADS# Issued during INIT: Case 2

Figure 4-7 assumes that an I/O cycle was used to generate the **INIT,** but the system waited until all bus activity had stopped (by monitoring the HALT special cycle) before asserting the **INIT** pin. In this case, the processor recognizes **INIT,** and starts a prefetch before **INIT** is deasserted. The prefetch may be from any location, and not necessarily the F..F0h address, even though **INIT** has been recognized.

On other Intel486 write through cache processors (Write-Back Enhanced IntelDX2 in standard bus mode and SL-Enhanced CPUs), the **SRESET** pin is executed immediately, in a manner similar to the **RESET** pin. This means that no cycles will be run after **SRESET** is asserted on these processors. With the Pentium OverDrive processor, it is the responsibility of the system to ensure that any cycles that are issued while INIT is active are completed properly to prevent data corruption, lost bus cycles or system lock-ups.

4.4 Instruction Prefetch

The Pentium OverDrive processor contains a prefetch buffer of several bytes, and can prefetch a significant number of bytes beyond the end of the last executed instruction. In addition, the processor implements a dynamic branch prediction algorithm which speculatively runs code fetch cycles to addresses corresponding to instructions executed some time in the past. Such code fetch cycles are run based on past execution history, regardless of whether the instructions retrieved are relevant to the currently executing instruction sequence.

The effect of both mechanisms is that the Pentium OverDrive processor may run code fetch bus cycles to retrieve instructions which are never executed. Although the opcodes retrieved are discarded, the system must complete the code fetch bus cycle by returning **RDY#/BRDY#.** It is particularly important that the system return **RDY#/BRDY#** for all code fetch cycles, regardless of the address.

Furthermore, it is possible that the processor may run speculative code fetch cycles to addresses beyond the end of the current code segment. Although the processor may prefetch beyond the CS limit, it will not attempt to execute beyond the CS limit, it will raise a GP fault instead. Thus, segmentation cannot be used to prevent speculative code fetches to inaccessible areas of memory. On the other hand, the processor will never run code fetch cycles to inaccessible pages, so the paging mechanism guards against both the fetch and execution of instructions in inaccessible pages.

If the processor has been placed in a halt state with the **HLT** instruction, and the processor has issued the halt cycle, or the processor has run a shutdown cycle, one of the methods of exiting this condition is to assert an interrupt. Once the interrupt is asserted, the Pentium OverDrive processor may issue a prefetch before the interrupt is acknowledged with an interrupt cycle, or the action desired by the interrupt is performed. For example, if the processor is in a halt state, and the **FLUSH#** interrupt is asserted, the processor could exit the halt state, perform a prefetch, and then start driving the write backs for the flush operation. Prefetches of this type may be run after any interrupt, including **INTR.**

For memory reads and writes, both segmentation and paging prevent the generation of bus cycles to inaccessible regions of memory.

5.0 SOFTWARE CONSIDERATIONS

5.1 External Bus Cycle Ordering

5.1.1 WRITE BUFFERS AND MEMORY ORDERING

The Pentium OverDrive processor has write buffers to enhance the performance of consecutive writes to memory. Writes in these buffers are driven out on the external bus in the order they were generated by the processor core. No reads (as a result of cache miss) are reordered around previously generated writes sitting in the write buffers (Unlike the IntelDX2 processor). The implication of this is that the write buffers will be emptied before a subsequent processor generated bus cycle is run on the external bus.

It should be noted that only memory writes are buffered and I/O writes are not. There is no guarantee of synchronization between completion of memory writes on the bus and instruction execution after the write. The OUT instruction or a serializing instruction needs to be executed to synchronize writes with the next instruction. Please refer to the *Pentium Processor Programmers Reference Manual* for information on serializing instructions.

No re-ordering of read cycles occurs on the Pentium OverDrive processor. Specifically, the write buffers are emptied before the IN instruction is executed.

5.1.2 EXTERNAL EVENT SYNCHRONIZATION

When the value of **NMI, INTR, FLUSH#, SMI#** or **INIT** changes as the result of executing an OUT instruction, these inputs must be at a valid state three clocks before **RDY#/BRDY#** is returned to ensure that the new value will be recognized before the next instruction is executed.

Note that if an OUT instruction is used to modify **A20M#,** this will not affect previously prefetched instructions. A serializing instruction must be executed to guarantee recognition of **A20M#** before a specific instruction.

5.2 Model Specific Registers

The Pentium OverDrive processor defines certain Model Specific Registers that are used in execution tracing, performance monitoring and testing. They are unique to the Pentium OverDrive processor and may or may not be implemented in the same way in future processors.

Please contact Intel for more information on the model specific registers.

5.3 Exception Priorities

Exceptions are serviced and recognized on the boundary between instructions. The instruction pointer pushed onto the stack for the interrupt handler points to the next instruction. The priority among simultaneous exceptions is as follows (interrupt vector numbers are shown in decimal in parentheses):

Trap on the previous instruction:

- Breakpoint (#3)

External Interrupts:

- **FLUSH#**
- **SMI#**
- **INIT**
- **NMI**
- **INTR**

Floating Point Errors:

- **FERR#**

External Interrupt:

- **STPCLK#**

Faults on Fetching Next Instruction:

- Code Seg Limit Violation (#13), Page Fault on prefetch (#14) (the relative priority unpredictable)

Faults in Decoding the next Instruction:

- Invalid Opcode (#6), Device Not Available (#7)
- General Protection Fault for Instruction Length > 15B (#13)

Faults on Executing an Instruction (These may occur in a manner that varies from implementation to implementation as necessary to insure functional correctness. They are not listed in any particular order):

- General Detect (#1)
- FP Error (from previous FP instruction) (#16)
- Interrupt on Overflow (#4)
- Bound (#5)
- Invalid TSS (#10)
- Segment Not Present (#11)
- Stack Exception (#12)
- General Protection (#13)
- Data Page Fault (#14)
- Alignment Check (#17)

5.3.1 EXTERNAL INTERRUPT CONSIDERATIONS

The Pentium OverDrive processor recognizes the following external interrupts: **FLUSH#, SMI#, INIT, NMI, INTR** and **STPCLK#.** They are listed in priority order, however, they are subject to the considerations listed below.

FLUSH#

Note that unlike the Intel486 CPU which invalidates its cache a small fixed number of clocks after **FLUSH#** is asserted, the **FLUSH#** pin on the Pentium OverDrive processor is an interrupt and therefore is only recognized at the boundary between instructions. While **FLUSH#** is being serviced, all the dirty lines in the data cache are written back to main memory. This may take several thousand clocks. During this time no instructions are executed and no other interrupts are recognized. If the processor is in the HALT or Shutdown state, **FLUSH#** is still recognized. The processor will return to the HALT or Shutdown state after servicing the **FLUSH#.**

5.4 BIOS and Software

The following should be considered when designing a Pentium OverDrive processor based system.

5.4.1 Pentium® OverDrive® PROCESSOR DETECTION

The component identifier and stepping/revision identifier for the Pentium OverDrive processor is readable in the DX register immediately after RESET, where

DX = 153xh

The x can be any value from 0 to Fh and refers to the stepping of the part.

As with the IntelDX2 microprocessor specification, it is recommended that the BIOS save the contents of the DX register, immediately after RESET, so that this information can be used later, if required.

Software can also find out the component identifier and stepping/revision by invoking the CPUID instruction.

5.4.2 BIOS BOOT CODE ASSUMPTIONS

In preliminary tests with systems that support the Pentium OverDrive processor, it was found that the aggressive prefetch unit of the processor would attempt to fetch from the x0 . . . 00h address after a **RESET.** Since this address exists in real memory and the BIOS had not been able to properly initialize it before this point, parity errors would be detected by the system.

To avoid issue, the Pentium OverDrive processor prefetch unit is disabled any time the processor is restarted with **RESET** to prevent the prefetcher from attempting to fetch code from address x0..00h after wrapping around from xF..FFh. In the sixteen bytes from xF..F0h to xF..FFh, there must be at least one jump instruction (of any type) that transfers code execution out of the xF..F0h to xF..FFh region. If not, the Pentium OverDrive processor will not enable the prefetch unit, and processor operation will stop.

INIT does not place this restriction on the prefetcher since it is assumed that parity will have been initialized in the main memory before **INIT** is executed.

5.4.3 TIMING DEPENDENT LOOPS AND BIOS

The Pentium OverDrive processor executes instructions at a frequency which is a multiple of the bus frequency. The Pentium OverDrive processor also uses advanced design techniques to decrease the number of clocks per instruction (CPI) from that of the Intel486 processors. Thus, software such as instruction based timing loops will execute faster on the Pentium OverDrive processor than on the Intel486 processors at the same bus frequency. Instructions such as NOP, LOOP, and JMP $+2, are frequently used by BIOS to implement timing loops, that are required, for example, to enforce recovery time between consecutive accesses for I/O devices. These instruction based timing loop implementations may require modification to be compatible with the Pentium OverDrive processor.

In order to avoid any incompatibilities, it is recommended that timing loops be implemented in hardware rather than in software. This provides transparency and also does not require any change in BIOS or I/O device drivers in the future when moving to higher processor clock speeds.

As an example, a timing loop may be implemented as follows: The software performs a dummy I/O instruction to an unused I/O port. The hardware for the bus controller logic recognizes this I/O instruction and delays the termination of the I/O cycle to the CPU by keeping **RDY#** or **BRDY#** deasserted for the appropriate amount of time.

5.4.4 TEST REGISTER ACCESS

The IntelDX2 processor has test registers which allow OEM's to test the functionality of different areas of the component. These test registers are accessed on the Intel486 processor family using the "MOV reg, TRx and MOV TRx, reg" instructions. These instructions are not available on the Pentium OverDrive processor. Any attempt to execute them will cause a invalid opcode exception. The Pentium OverDrive processor uses the Model Specific Registers (MSR's) to implement on chip testing. These MSR's are accessed using the RDMSR and WRMSR instructions. BIOS must recognize this fundamental difference between the Pentium OverDrive processor and the IntelDX2 processor and act accordingly.

6.0 DIFFERENCES BETWEEN THE Intel486 FAMILY AND THE Pentium® OverDrive® PROCESSOR

This section covers the differences between the Intel486 family of microprocessors and the Pentium OverDrive processor.

6.1 Software

The Pentium OverDrive processor is compatible with the entire installed base of applications for MS-DOS*, Windows*, OS/2*, and UNIX*. In addition to being binary compatible with the Intel architecture based processors which preceded the Pentium processor, it can also run programs which have been compiled to utilize Pentium processor instructions. This allows pairing of instructions to take advantage of the Superscalar Architecture and adds floating point instructions if replacing an Intel486 SX or IntelSX2 processor.

6.2 Hardware

The Pentium OverDrive processor is in a 237-Pin Grid Array package while the Intel486 family uses a 168-Pin Grid Array package. These extra pins are used for extra power and ground pins, including separate power and ground for the fan heatsink, also the internal cache write-back signals are on these pins.

7.0 DIFFERENCES BETWEEN THE Pentium® PROCESSOR AND THE Pentium® OverDrive® PROCESSOR

There are several differences between the Pentium processor and the Pentium OverDrive processors. These differences are covered in the next two sections.

7.1 Software

The following paragraphs are provided as a reference for software differences between the Pentium OverDrive processor and the Pentium processor. Unless otherwise stated, it can be assumed that the Pentium OverDrive processor will have the same software characteristics as the Pentium processor. For more information on the software characteristics of the Pentium Processor, please see the *Pentium Processor Data Book* or *Programmers Reference Manual*.

The Pentium OverDrive processor does not support machine check exception. As a result, CR4.MCE is not useful. It will be forced to a zero by the hardware. However, any attempt by the software to set this bit to 1 will not create a general protection exception.

The Pentium OverDrive processor allows two different page sizes: 4 KB and 4 MB. Please contact Intel for more information on the use of 4 MB pages.

The behavior of INVD, WBINVD and INVPLG instructions are similar to the Pentium processor. If the processor is in **the enhanced bus mode,** the WBINVD instruction will write back all dirty lines first, flush the cache and run two special cycles (the write back special cycle followed by the flush special cycle) on the bus. INVD will flush the cache and run one special cycle (The flush special cycle) on the bus. INVD will not write back the dirty lines, if any. All three instructions are privileged level 0 and should be executed by BIOS or operating system code only.

On the IntelDX2 processor, when paging is disabled, and/or when instructions that are not affected by paging are executed, the **PCD** and **PWT** pins are driven with values from CR3.PCD and CR3.PWT bits, respectively. On the Pentium OverDrive processor, when paging is disabled and/or when instructions that are not affected by paging are executed, the **PWT** pin will be drive LOW and the **PCD** pin will reflect the value of the CR0.CD bit.

When the CPUID instruction is performed with EAX = 1, the Pentium OverDrive processor will return the following values to the EDX register. These bits indicate what the features of the processor are.

The various bit positions have the following meaning:

Table 7-1. Feature Bit Assignment

Bit	Value	Meaning
0	1	FPU: Floating Point Unit On-Chip
1	1	VME: Virtual-8086 Mode Enhancements
2	1	DE: Debugging Extensions
3	1	PSE: Page Size Extension
4	1	TSC: Time Stamp Counter
5	1	MSR: Pentium Processor-Style MSR
6	R	Reserved
7	R	Reserved
8	1	CX8: CMPXCHG8B Instruction
9–31	R	Reserved

A value of "R" means that the corresponding bit is reserved and the software should not depend on its value.

7.2 Hardware

This section covers the hardware differences between the Pentium processor and the Pentium OverDrive processor.

The Pentium processor has a 64-bit data bus while the Pentium OverDrive processor has a 32-bit data bus. This is required in order for the Pentium OverDrive processor to work in an Intel486 architecture based system.

The size of the data bus requires a similar decrease in the internal cache line size. A burst memory access is four bus widths of data this is the length of each line in the cache. For an Intel486 based architecture system that is 16-Bytes, for a Pentium processor based system this is 32-bytes. The internal cache in the Pentium processor is expecting 32-bytes. This would require two burst reads. Therefore the cache line size was reduced to 16-bytes wide.

The cache on the Pentium processor is split into two 8 KByte caches. One is for data and the other is the instruction or code cache. The Pentium OverDrive processor keeps the idea of two separate caches but increases the size to 16 KBytes each.

The Pentium OverDrive processor does not have the JTAG boundry scan capabilities that the Pentium processor has.

The package is different. The Pentium processor is packaged in a 273-Pin Grid Array while the Pentium OverDrive processor uses a 237-Pin Grid Array package.

The Pentium OverDrive processor has the integrated fan heatsink attached. This integrated fan informs the processor if the fan has slowed or stopped. This reduces the internal frequency to 1x multiplier from the previous 2.5x. The part can run indefinitely at the lower frequency without incurring any damage. This allows the Pentium OverDrive processor to continue in the system until a replacement fan can be installed.

8.0 TESTABILITY

8.1 Introduction

This section describes the features which are included in the Pentium OverDrive processor for the purpose of enhancing the testability of the part. The capabilities of the Intel486 processor test hooks are included in the processor, however they are implemented differently. In addition, new test features were added to assure timely testing and production of a system product. All features described here are also present in the Pentium processor.

Internal component testing through the Built In Self Test (BIST) feature of the Pentium OverDrive processor provides 100% single stuck at fault coverage of the microcode ROM and large PLAs. Some testing of the instruction cache, data cache, Translation Lookaside Buffers (TLBs), and Branch Target Buffer (BTB) is also performed. In addition, the constant ROMs are checked.

The production version of the Pentium OverDrive processor will not include the boundary scan or testability pins.

Several test registers are also included in the Pentium OverDrive processor to simplify access to all on-chip caches and TLBs. These test registers on the processor are not compatible with the definitions for

Table 8-1. Pentium® OverDrive® Processor RESET Modes

RESET	INIT	Type of Reset	Effect on I/D Caches	Effect on FP Registers	Effect on SMM Base Register
0	0	None	Not Applicable	Not Applicable	Not Applicable
0	1	Warm Reset	None	None	None
1	X	Cold Reset (w/ BIST)	Invalidated	Initialized	Invalidated
1	X	Cold Reset (w/o BIST)	Invalidated	Undefined	Invalidated

the test registers on the IntelDX2 processor, and will be provided by Intel at a later date. For the latest information on these test registers, please contact Intel.

The following list summarizes the Pentium OverDrive processor testability features:

- Built In Self Test
- Cache and TLB Test Registers
- Tristate Test Mode

8.2 Pentium® OverDrive® Processor Reset Pins/BIST Initiation

Two pins, **RESET** and **INIT,** are used to reset the Pentium OverDrive processor in different manners. The following table shows the different types of resets that can be initiated using these pins.

Toggling either the **RESET** pin or the **INIT** pin individually forces the Pentium OverDrive processor to begin execution at address 0FFFFFFF0h. The internal instruction cache and data cache are invalidated when **RESET** is asserted (modified lines in the data cache are NOT written back). The instruction cache and data cache are not altered when the INIT pin is asserted without **RESET.** In neither case are the floating point registers altered. In both cases, the BTB, the segment descriptor cache and both TLBs are all invalidated.

Reset with self test is initiated by holding the **AHOLD** pin HIGH for 2 clocks before and 2 clocks after **RESET** is driven from HIGH to LOW. The instruction cache and data cache are invalidated and the floating point registers are initialized. The processor begins execution at address 0xFFFFFFF0h. The BTB, the segment descriptor cache and both TLBs are all invalidated before execution begins.

At the conclusion of reset, with or without self test, the DX register will contain a component identifier. The upper byte will contain 15h and the lower byte will contain a stepping identifier.

Table 8-2 defines the processor state after **RESET, INIT** and **RESET** with BIST (built in self test).

Table 8-2. Register State after RESET, INIT and BIST
(Register States are given in Hexadecimal Format)

Storage Element	RESET (no BIST)	RESET (BIST)	INIT
EAX	0	0 if pass	0
EDX	1530 + stepping	1530 + stepping	1530 + stepping
ECX, EBX, ESP EBP, ESI, EDI	0	0	0
EFLAGS	2	2	2
EIP	0FFF0	0FFF0	0FFF0
CS	selector = F000	selector = F000	selector = F000
	base = FFFF0000	base = FFFF0000	base = FFFF0000
	limit = FFFF	limit = FFFF	limit = FFFF

Table 8-2. Register State after RESET, INIT and BIST
(Register States are given in Hexadecimal Format) (Continued)

Storage Element	RESET (no BIST)	RESET (BIST)	INIT
DS,ES,FE,GS,SS	selector = 0	selector = 0	selector = 0
	base = 0	base = 0	base = 0
	limit = FFFF	limit = FFFF	limit = FFFF
IDTR	base=0	base=0	base=0
	limit=FFF	limit=FFF	limit=FFF
GDTR,LDTR,TR	undefined	undefined	undefined
CR0	60000010	60000010	Note 1
CR2,3,4	0	0	0
DR3-0	0	0	0
DR6	FFFF0FF0	FFFF0FF0	FFFF0FF0
DR7	00000400	00000400	00000400
Time Stamp Counter	0	0	UNCHANGED
Control and Event Select	0	0	UNCHANGED
TR12	0	0	UNCHANGED
All Other MSR's	undefined	undefined	UNCHANGED
CW	undefined	37F	UNCHANGED
SW	undefined	0	UNCHANGED
TW	undefined	FFFF	UNCHANGED
FIP,FEA,FCS, FDS,FOP	undefined	0	UNCHANGED
FSTACK	undefined	undefined	UNCHANGED
Data and Code Cache	invalid	invalid	UNCHANGED
Code Cache TLB, Data Cache TLB, BTB, SDC	invalid	invalid	invalid

NOTE:
1. CD and NW are unchanged, bit 4 is set to 1, all other bits are cleared.
   State of output pins after RESET:
   High: **LOCK#, ADS#, PCHK#, HIT#, HITM#, FERR#, SMIACT#**
   Low: **HLDA, BREQ**
   High Impedance: **D31-D0**
   Undefined: **A31-A3, BE3#-BE0#, W/R#, M/IO#, D/C#, PCD, PWT, CACHE#**

8.3 Built In Self Test (BIST)

Self test is initiated by holding the **AHOLD** pin HIGH for the clock before **RESET** changes from HIGH to LOW. If asserted asynchronously, AHOLD must be asserted two clocks before and two clocks after **RESET** to guarantee recognition.

No bus cycles are run by the Pentium OverDrive processor during self test. The duration of self test is approximately 2^{19} internal clocks. Approximately 70% of the devices in the processor are tested by BIST.

The Pentium OverDrive processor BIST consists of two parts: hardware self test and microcode self test.

During the hardware portion of BIST, the microcode and all large PLAs are tested. All possible input combinations of the microcode ROM and PLAs are tested.

The constant ROMs, BTB, TLBs, and all caches are tested by the microcode portion of BIST. The array tests (caches, TLBs, and BTB) have two passes. On the first pass, data patterns are written to arrays, read back and checked for mismatches. The second pass writes the complement of the initial data pattern, reads it back, and checks for mismatches. The constant ROMs are tested by using the microcode to add various constants and check the result against a stored value.

Upon completion of BIST, the cumulative result of all tests are stored in the EAX register. If EAX contains 0x0h, then all checks passed; any non-zero result indicates a faulty unit.

During BIST, **EADS#** should not be used to perform snoops, otherwise false **HITM#** indications, with no corresponding write back cycles, can occur.

8.4 Tri-State Test Mode

The Pentium OverDrive processor provides the ability to float all its outputs and bi-directional pins. This includes pins that are floated during bus hold as well as some pins that are not normally floated during normal operation. When the Pentium OverDrive processor is in tri-state test mode, external testing can be used to test on board connections.

The tri-state test mode is invoked by driving **FLUSH#** low for 2 clocks before and 2 clocks after **RESET** going low. The outputs are guaranteed to tri-state no later than 10 clocks after **RESET** goes low. The processor will remain in tri-state test mode until the next **RESET.**

8.5 Cache, TLB and BTB Test Registers

The Pentium OverDrive processor contains several test registers. The purpose of the test registers is to provide direct access to the processor caches, TLBs, and BTB, so user programs can easily exercise these structures. Because the architecture of the caches, TLBs, and BTB is different, a different set of test registers (along with a different test mechanism) is required for each. Most test registers can be shared between the code and data caches.

Since much of the testability hardware is used for other purposes during normal operation of the Pentium OverDrive processor, some restrictions may exist on what software may do while testability operations are being run.

Please contact Intel for more information on the Pentium OverDrive processor Cache, TLB, and BTB Test Registers.

8.6 Fan Protection Mechanism and THermal ERRor Bit

The Pentium OverDrive processor employs an active fan/heatsink unit to assist in cooling the processor. Another integral part of this cooling solution is the ability for software to poll the status of the fan to determine if the fan has fallen to a speed that is unacceptable to cool the processor. Should the fan fall into a speed range that is too slow, a control register will record the event. (For more information, please contact Intel.)

9.0 MECHANICAL AND ELECTRICAL DESIGN CONSIDERATIONS

9.1 Introduction

This section provides mechanical and electrical guidelines for designing a system to support the Pentium OverDrive processor. The layout considerations for the socket and spatial requirements for the Pentium OverDrive processor are discussed first, along with other mechanical issues. Sample circuits for support of the Pentium OverDrive processor in write back or write through cache mode are provided in the electrical section. Any design using the Pentium OverDrive processor must take the thermal considerations of the processor into account as well. To this end, thermal design numbers and calculations for the fan/heatsink unit are also provided.

9.2 Mechanical Design Considerations

This section discusses the mechanical design considerations for the Pentium OverDrive processor, including dimensions and the active heat sink unit.

9.2.1 PHYSICAL DIMENSIONS

The Pentium OverDrive processor is designed to fit in a standard 240-lead (19 x 19) PGA socket with four corner pins removed. The Pentium OverDrive processor will use an active heat sink, and therefore requires more vertical clearance. For more discussion on the Pentium OverDrive processor active heat sink, please see the following section.

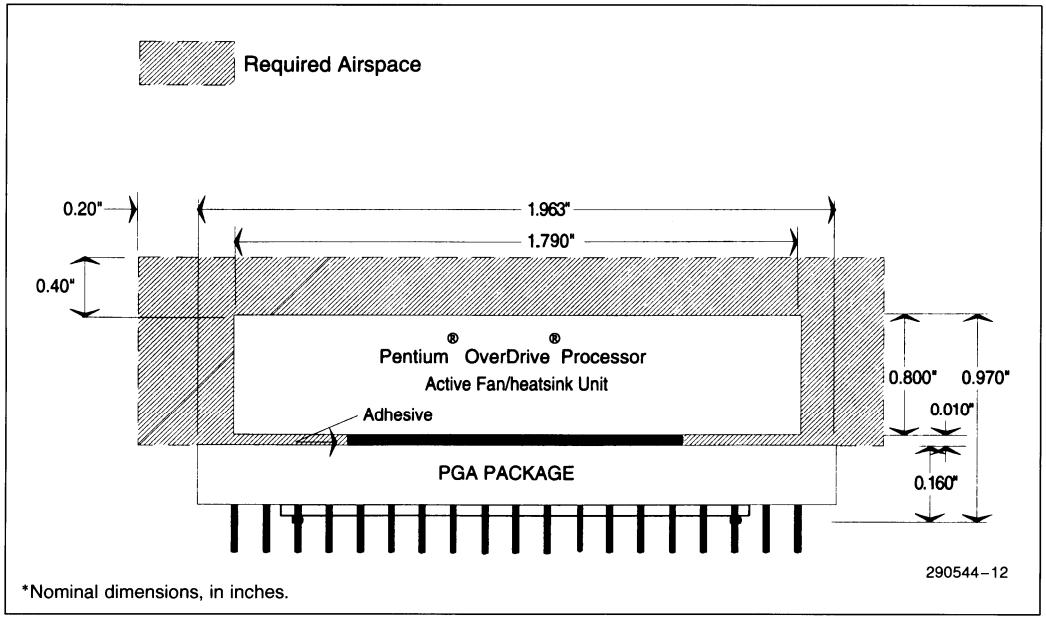
The maximum and minimum dimensions of the Pentium OverDrive processor package with the active heat sink are shown in Table 9-1. The active heat sink unit is divided into the size of the actual heat sink, and the required free space above the heat sink. The total height required for the Pentium OverDrive processor from the motherboard will depend on the height of the PGA socket. The total external height given in the table below is only measured from the PGA pin stand-offs. Table 9-1 also details the minimum clearance needed around the PGA package.

Table 9-1. Pentium® OverDrive® Processor, 235-Pin, PGA Package Dimensions with Active Heat Sink Attached

Component (inches)	Length and Width		Height	
	Min	Max	Min	Max
PGA Package	1.950	1.975	0.140	0.180
Adhesive	N/A	N/A	0.008	0.012
Fan/Heat Sink	1.77	1.82	0.790	0.810
Required Airspace	0.200	N/A	0.400	N/A
External Pkg. Total	1.950	1.975	0.938	1.002
Min. Ext. w/ Airspace Fixture	2.150		1.338	

9.2.2 ACTIVE HEAT SINK DETAILS

Since the Pentium OverDrive processor dissipates more power than the Intel486 Family, it requires a larger cooling capacity. To accomplish the task of cooling the Pentium OverDrive processor, an active heat sink is attached to the top of the part. The active heat sink will use a heatsink/fan combination to provide airflow at high velocity to the Pentium OverDrive



*Nominal dimensions, in inches.

Figure 9-1. 235-Pin, PGA Package with Active Heat Sink Attached

processor. No external connections (Power, etc . . .) will be required for the active heat sink. All the needed connections will be made through the pins of the processor. The amount of extra power needed for the fan is taken into account in the I_{CC} numbers of the processor.

The fan/heatsink unit also supports an integrated thermal protection mechanism that will allow the fan to signal the processor if the speed of the fan should become insufficient to cool the processor. Should this occur, the processor will modify its internal core frequency to match the **CLK** input in a manner that is transparent to the external system. The fan/heatsink has been designed so that should the fan stop, it will have the capability to properly cool the processor in a still air environment. The fan unit is removable so that the unit may be easily replaced. If the fan is removed, or power to the fan is lost, the processor will treat these conditions as if the fan has failed. Figure 9-2 below gives a functional representation of the Pentium OverDrive processor and heat sink unit.

As can be seen in the mechanical dimensions in Table 9-1, the actual height required by the heat sink is less than the total space allotted. Since the Pentium OverDrive processor employs an active heat sink, a certain amount of space is required above the heat sink unit to ensure that the airflow is not blocked. Figure 9-3 shows unacceptable blocking of the airflow for the Pentium OverDrive processor heat sink unit. Figure 9-4 details the minimum space needed around the PGA package to ensure proper heat sink airflow.

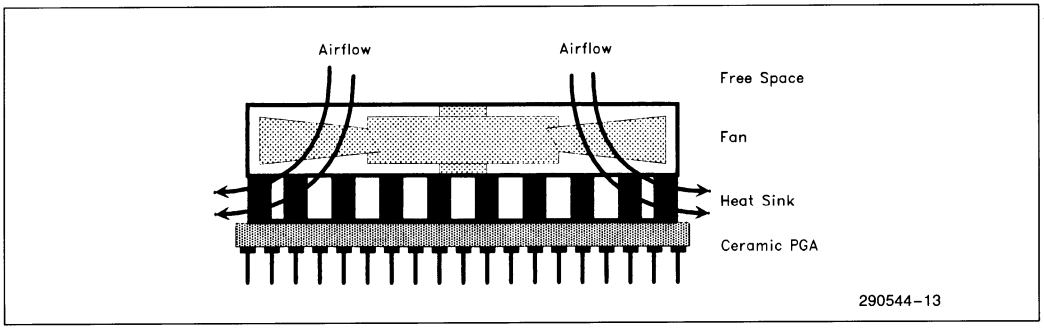


Figure 9-2. Active Heat Sink Example

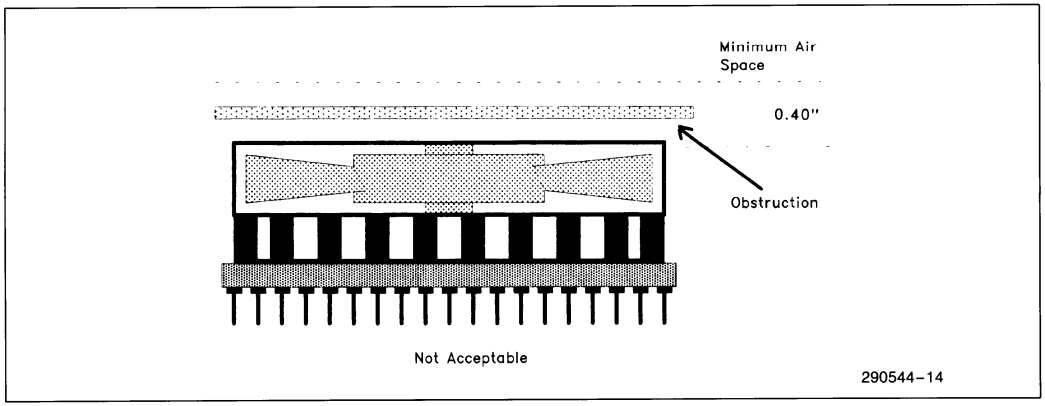


Figure 9-3. Active Heat Sink Top Space Requirements

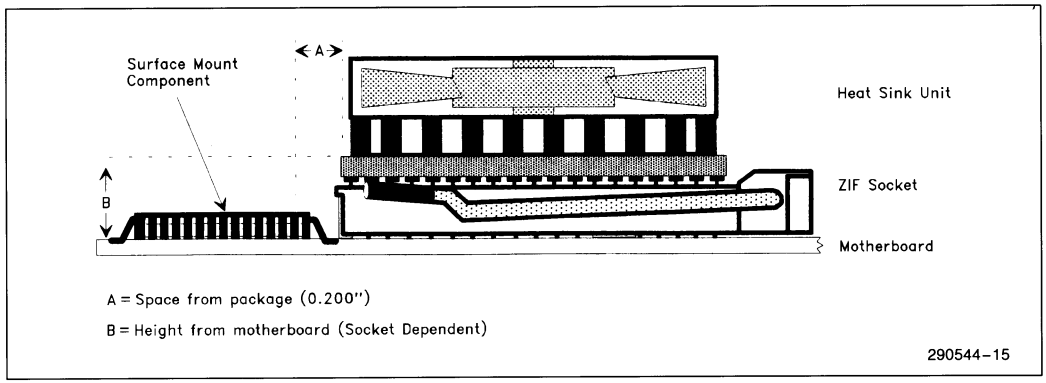


Figure 9-4. Required Free Space from Sides of PGA Package

As shown in Figure 9-4, it is acceptable to allow any device to enter within the free space distance of 0.2″ from the PGA package if it is not taller than the level of the heat sink base. In other words, if a component is taller than height "B", it can not be closer to the PGA package than distance "A". This applies to all four sides of the PGA package, although the back and handle sides of a ZIF socket will generally automatically meet this specification since they have widths larger than distance "A".

9.2.3 SOCKET 3 PINOUT

Socket 3 is the ZIF (Zero Insertion Force) socket recommended for the Pentium OverDrive processor. To ensure proper orientation, four corner pins have been removed from the outer row of pins. This includes the "key" pin in the inside corner. Figure 9-5 shows an example of the pinout of Socket 3.

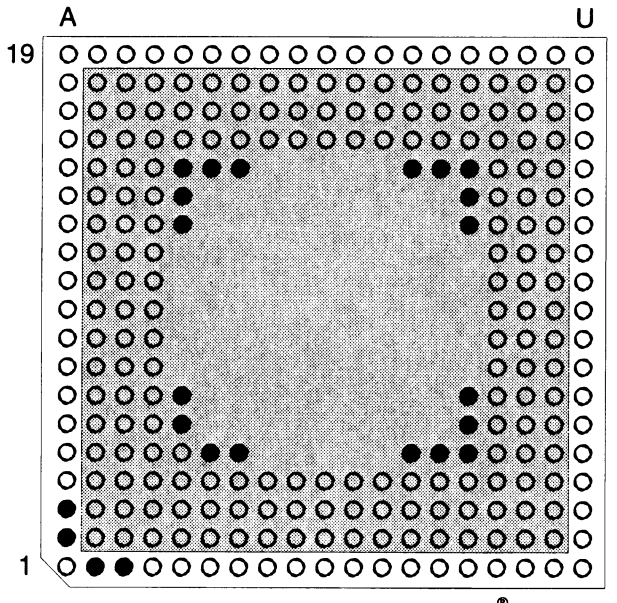


Figure 9-5. 237-Pin, PGA ZIF Socket 3

Product Highlights

- Distinctive socket with the "Socket 3" marking
- Rapid end user access to Socket 3
- Keyed ZIF socket for easy and correct Pentium OverDrive processor installation

9.2.4 "END USER EASY" RECOMMENDATIONS

PC buyers value easy and safe upgrade installation. PC manufacturers can make upgrade component installation in the Pentium OverDrive processor socket simple and foolproof for the end user and reseller by implementing the suggestions listed in Table 9-2. These are presented here as strong guidelines for any Pentium OverDrive processor design.

Table 9-2. Socket and Layout Considerations

"End User Easy" Feature	Implementation
Visible Pentium OverDrive Processor Socket	The Pentium OverDrive processor socket should be easily visible when the PC's cover is removed. Label the Pentium OverDrive Processor socket and the location of pin 1 by silk screening this information on the PC board.
Accessible Pentium OverDrive Processor Socket	Make the Pentium OverDrive processor socket easily accessible to the end user. (e.g., do not place the Pentium OverDrive processor socket under a disk drive.) Be sure to leave enough clearance to open the Zero Insertion Force (ZIF) socket.
Foolproof Chip Orientation	The Pentium OverDrive processor socket must insure proper orientation of the Pentium OverDrive processor. The 236-pin, PGA package of the Pentium OverDrive processor is orientated by the four corner pins that have been removed from the "pin 1" corner. These four contacts (A2, A3, B1, and C1) in the socket should be plugged, such that PGA pins cannot be inserted, to assure correct orientation. All inside contacts (11 innermost rows) should be plugged, except the "key" pin (E5), to insure correct orientation and alignment. The total number of contacts fo the Pentium OverDrive processor socket is therefore 237; a standard 240-pin socket plus the inside "key" pin and less the four outside corner pins. Supplying a 237-pin socket as the Pentium OverDrive processor socket eliminates the possibility of end users or resellers damaging the PC board or the Pentium OverDrive processor by powering up the system with the Pentium OverDrive processor in the incorrect orientation.
Zero Insertion Force Pentium OverDrive Processor Socket	The high pin count of the Pentium OverDrive processor makes the insertion force required for installation into a screw machine PGA socket excessive. Even most Low Insertion Force (LIF) sockets require more than 60 lbs. of insertion force. A Zero Insertion Force (ZIF) socket insures that the chip insertion force does not damage the PC board. Be sure to allow enough clearance for the ZIF socket handle. Do not use a LIF or screw machine socket.
"Plug and Play"	Jumper or switch changes should not be needed to electrically configure the system for the Pentium OverDrive processor.
Thorough Documentation	Describe the Pentium OverDrive processor socket and the Pentium OverDrive processor installation procedure in the PC's User's Manual.

9.2.6 ZIF SOCKET VENDORS

Intel can provide a complete list of socket manufacturers that have been qualified to produce Socket 3. For more information, please contact your local Intel sales office.

9.3 Upgrade Circuit Design

9.3.1 DUAL PROCESSOR SITE DESIGN

The Pentium OverDrive processor can reside on the same processor bus as an Intel486 processors. The Pentium OverDrive processor specifies a **UP#** output (Upgrade Present) pin which should be connected directly to the **UP#** input pin of the Intel486 microprocessor. When the Pentium OverDrive processor occupies the Pentium OverDrive processor socket, the UP# signal (active low) forces the Intel486 microprocessor to tri-state all outputs and reduce power consumption. When the Pentium OverDrive processor is not present, a pull-up resistor, internal to the Intel486 microprocessor, drives **UP#** inactive and allows the Intel486 microprocessor to control the processor bus.

9.3.2 SINGLE PROCESSOR SITE DESIGN

A single processor site is defined as a system design that can accept all Intel486 processors in a single socket location. Doing a single socket design requires that certain pins are connected via the **INC** pins of the Pentium OverDrive processor. See Section 9 for more details on how to design a single socket processor site compatible other Intel486 processors.

9.3.3 CIRCUIT CONSIDERATIONS FOR WRITE BACK CACHE SUPPORT

The Pentium OverDrive processor is specified to support the MESI write back protocol for the on-chip cache. To support the write back protocol, seven new signals , are defined for the Pentium OverDrive processor, four of which are present on the Write-Back Enhanced IntelDX2 processor. The new signals defined for MESI write back capability are **WB/WT#, INV, HIT#, HITM#, CACHE#, EWBE#,** and **BLEN#**. Another new pin, **INIT,** is used to facilitate warm resets. These new signals are defined in detail in Section 2. For more information on designing a system for processor write back cache support that is compatible with the Write-Back Enhanced IntelDX2 processor, please see Section 10.

9.3.4 Pentium® OverDrive® PROCESSOR DECOUPLING CAPACITORS

Because of the fast internal switching speeds of the Pentium OverDrive processor, it is important that the Pentium OverDrive processor use a liberal amount of decoupling capacitors. For proper V_{CC} transient response, Intel recommends that a system design employ at least 4 each of 47 μF bulk capacitors and 9 each of 0.1 μF and 0.01 μF capacitors. It is recommended that surface mount capacitors be used for decoupling the Pentium OverDrive processor. This style of capacitor introduces less inductance than leaded capacitors, so fewer are needed to achieve the same results. The capacitors should be added around the Pentium OverDrive processor in a manner that ensures they are evenly spread about and close to the processor location.

9.4 Socket Test Requirements

The electrical functionality of the Pentium OverDrive processor socket can be verified by fully testing the PC with a populated Pentium OverDrive processor socket. The Pentium OverDrive processor should be used to test for hardware and software compatibility. The BIOS requirements to maintain compatibility with all OverDrive processors are discussed in the Implementation Speicific Details section of the Pentium OverDrive processor Specification. All OverDrive processors undergo thorough application software compatibility testing prior to their introduction. If the system design supports a write back processor cache, the design should be tested with the Write-Back Enchanced IntelDX2 processor as well.

9.5 Thermal Management

The Pentium OverDrive processor and system chassis have several unique design requirements due to the attached active heat sink. The following sections provide sample maximum system operating temperature calculations so that systems may be designed to comply with the thermal requirements of the Pentium OverDrive processor.

9.5.1 THERMAL CALCULATIONS FOR A HYPOTHETICAL SYSTEM

The following equation can be used to calculate the maximum operating temperature of a system.

$T_{A(IN)} = T_{SINK} - (Power * \theta_{SI})$

The parameters are defined as follows:

$T_{A(IN)}$: The temperature of the air going **into** the heat sink fan unit.

T_{SINK}: Temperature of heat sink base, as measured in the center.

Power: Dissipation in Watts = $V_{CC} * I_{CC}$

θ_{SI}: Heat Sink to Internal Temperature [$T_{A(IN)}$] Thermal Resistance

$T_{A(OUT)}$: The temperature of the air outside the system.

Since the Pentium OverDrive processor uses an active heat sink, θ_{SI} is relatively constant, regardless of the airflow provided to the processor. The θ_{SI} is provided in Table 9-3. Table 9-4 details the maximum current requirements of the Pentium OverDrive processor. The maximum allowable $T_{A(IN)}$ is 55°C for both 25 MHz and 33 MHz with the heat sink attached.

Table 9-3. Thermal Resistance (°C/W) θ_{SI}

Processor Type	θ_{SI}—°C/W
Active Heat Sink	2.4

Table 9-4. Pentium® OverDrive® Processor Typical and Maximum I_{CC} Values

System Frequency (MHz)	Processor Typical I_{CC} (mA)	Processor Maximum I_{CC} (mA)
25	TBD	1900
33	TBD	2800

I_{CC} is dependent upon the V_{CC} level of the system, processor bus loading, software code sequences, and silicon process variations. For the Pentium OverDrive processor specifications, the maximum I_{CC} value is derived by testing a sample of components under the following worst case conditions: V_{CC} = 5.3V, full DC current loads on all output pins, and running a file with the predicted worst case software code sequences at the specified frequency. The typical I_{CC} value published is the I_{CC} corresponding to the worst observed I_{CC} value for an average component running under the above worst case conditions. No additional margin is added to this value. I_{CC} typical is not a guaranteed specification.

9.5.2 AIRFLOW

Since the Pentium OverDrive processor employs an active heat sink, it is not as important that the processor heat sink receive direct airflow, rather that the system has sufficient capability to remove the warm air that the Pentium OverDrive processor will generate. This implies that enough airflow exists at the Pentium OverDrive processor socket site to keep localized heating from occurring. This can be accomplished by a standard power supply fan with a clear path to the processor. Figure 9-6 shows how system design can cause localized heating to occur by limiting the airflow in the area of the processor. The airflow supplied in the system should also be enough to insure that the OEM processor shipped with the system will meet the OEM processor thermal specifications before the system is upgraded with the Pentium OverDrive processor.

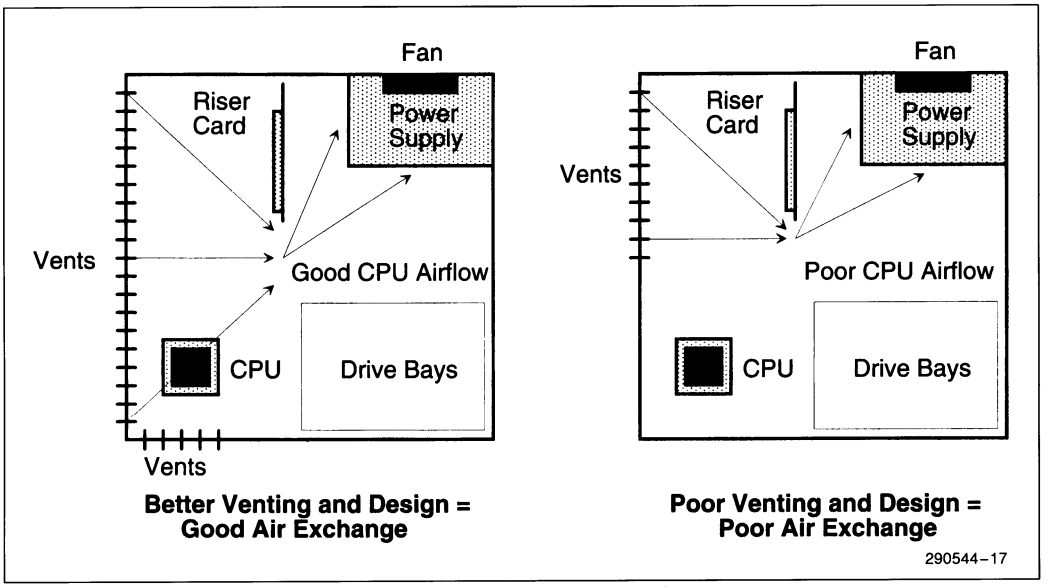


Figure 9-6. Pentium® OverDrive® Processor Airflow Design Examples

10.0 DESIGNING FOR Write-Back Enhanced IntelDX2/Pentium® OverDrive® PROCESSOR COMPATIBILITY

End Users have made upgradability an expected feature in any personal computer purchase. The Pentium OverDrive Processor is the intended upgrade for systems based on the Write-Back Enhanced IntelDX2 processor, an IntelDX2 processor with an on-board write back cache. When installed in a system designed to support a write back processor cache, the Pentium OverDrive processor can reach its full performance potential.

To make the task of designing an upgradable system easier, the Write-Back Enhanced IntelDX2 and the Pentium OverDrive processor have been designed to be compatible with one another. However, since the Pentium OverDrive processor retains many of its Pentium processor features, certain system design considerations must be taken into account to ensure that a Write-Back Enhanced IntelDX2 processor system can be upgraded seamlessly.

Throughout this section, a "Single Socket Design" will refer to a motherboard design that has only one processor site. This means that the Write-Back Enhanced IntelDX2 processor must be removed from the socket before the Pentium OverDrive processor can be installed. A "Dual Socket Design" refers to a two socket motherboard, one in which the Write-Back Enhanced IntelDX2 resides in a fixed location, and the Pentium OverDrive processor is installed into an empty upgrade socket. This section will make reference to both types of designs, but concentrates on the single socket design strategy.

The following section provides a list of considerations that must be examined to allow a Pentium OverDrive processor to operate properly in a system designed to support the Write-Back Enhanced IntelDX2 processor and a write back processor cache. The considerations listed here are only intended to be relevant to the Write-Back Enhanced IntelDX2 processor Enhanced Bus Mode although some may still be valid for the Standard Bus Mode. These considerations are provided as guidelines only, and should be used in conjunction with the rest of this document to ensure proper Pentium OverDrive processor operation.

10.1 Pinout Differences

The Pentium OverDrive processor pinout is based on a 19x19 PGA package as opposed to the Write-Back Enhanced IntelDX2 processor 17x17 PGA package. Most of the signals that are common between the Write-Back Enhanced IntelDX2 processor and the Pentium OverDrive processor exist on the same pin on both parts (assuming that pin A1 on the Write-Back Enhanced IntelDX2 processor = Pin B2 on the Pentium OverDrive processor).

NOTE:
All references to Pentium OverDrive processor pins are with respect to a 19x19 grid, while references to Write-Back Enhanced IntelDX2 processor pins are on a 17x17 grid.

10.1.1 ADDITIONAL PINS ON THE Pentium® OverDrive® PROCESSOR

The Pentium OverDrive processor defines signal pins that provide functionality that the Write-Back Enhanced IntelDX2 processor does not have. These pins are defined in Table 10-1 below.

Table 10-1. Additonal Pentium® OverDrive® Processor Pins

Signal Name	Pentium® OverDrive® Processor Pin/ Write-Back Enhanced IntelDX2 Processor Pin	Comment
BLEN# (Input)	A7/Not Present	**BLEN#** (Burst Length) controls write bursting on the Pentium OverDrive processor. It can not be toggled and should be tied high, low, or left unconnected. It must be driven LOW if the system is able to accept burst write backs. If **BLEN#** is driven HIGH to force write backs to be written out as four separate write cycles, HOLD will not be recognized until all four cycles have completed, even though each cycle will have its own **ADS#** and **BLAST#.**
EWBE# (Input)	P1/Not Present	**EWBE#** (External Write Buffer Empty) will allow writes to E or M state lines when asserted LOW. If it is sampled HIGH the processor will hold off writes to E or M state lines until asserted LOW again.
HIT# (Output)	U2/Not Present	**HIT#** provides an indication that an external snoop has hit a M,E or S state line in the internal cache.
UP# (Output)	C15/B14	**UP#** is driven LOW to indicate to the system that an upgrade processor is installed. In a single socket design, it shares a pin with the Write-Back Enhanced IntelDX2 processor signal, **TMS.** In a dual socket design, it should be connected to the Write-Back Enhanced IntelDX2 processor **UP#** (Input).

Due to its larger package and the ability to consume more power, the Pentium OverDrive processor also defines a number of extra V_{CC} and V_{SS} pins that the Write-Back Enhanced IntelDX2 processor does not support. The extra pins are listed in Table 10-2.

Table 10-2. Additional V_{CC} and V_{SS} Pins

V_{CC}	V_{SS}	V_{SS}	V_{CC}	V_{SS}	V_{SS}
	A5	U3	K19	G19	
A9	A8	U5	L1	H1	
A10	A12	U6	L19	H19	
A11	A13	U7	R1	M1	
A16	A14	U8	R19	M19	
D1	A15	U12	U4	N19	
D19	A17	U13	U9	Q1	
J1	C19	U14	U10	Q19	
J19	E1	U15	U11	S1	
K1	E19	U17	U16	S19	

10.1.2 PINS NOT SUPPORTED BY THE Pentium® OverDrive® PROCESSOR

The Pentium OverDrive processor supports all of the pins on the Write-Back Enhanced IntelDX2 processor except those required for JTAG boundary scan functionality and the **UP#** input pin. Single socket designs should ensure that if boundary scan features are implemented, they will not interfere with the operation of the Pentium OverDrive processor. Dual socket designs should not route the Pentium OverDrive processor into the boundary scan chain. Table 10-3 lists the location of the pins that exist on the Write-Back Enhanced IntelDX2 processor, and the corresponding different signals on the Pentium OverDrive processor.

Table 10-3. Unsupported Write-Back Enhanced IntelDX2 Processor Pins

Write-Back Enhanced IntelDX2 Processor Signal Name/Pin	Pentium® OverDrive® Processor Signal Name/Pin	Comment
TCK (Input) Pin A3	**INC** Pin B4	Pin B4 on the Pentium OverDrive processor is defined as an **INC** pin so that **TCK** can be used by the Write-Back Enhanced IntelDX2 processor in a single socket design without requiring a jumper.
TDI (Input) Pin A14	**INC** Pin B15	Pin B15 on the Pentium OverDrive processor is defined as an **INC** pin so that **TDI** can be used by the Write-Back Enhanced IntelDX2 processor in a single socket design without requiring a jumper.
TDO (Output) Pin B16	**INC** Pin C17	Pin C17 on the Pentium OverDrive processor is defined as an **INC** pin so that **TDO** can be used by the Write-Back Enhanced IntelDX2 processor in a single socket design without requiring a jumper.
TMS (Input) Pin B14	**UP#** (Output) Pin C15	If the Write-Back Enhanced IntelDX2 processor boundary scan features are used in a single socket design, the design should ensure that **TMS** will not conflict with the Pentium OverDrive processor **UP#** when the upgrade is installed.
UP# (Input) Pin C11	**INC** Pin D12	Pin D12 on the Pentium OverDrive Processor is defined as an **INC** pin so that there can be no conflict with **UP#** (Input).

10.1.3 SHARED SIGNALS LOCATED ON DIFFERENT PINS

There are several signals that the Pentium OverDrive Processor has in common with the Write-Back Enhanced IntelDX2 processor, but which are located on different pins. An example of this would be the **HITM#** signal. On the Pentium OverDrive processor, it is located in the outer row of pins, while on the Write-Back Enhanced IntelDX2 processor, it is located on one of the inner row processors. Single socket designs require that these signals be tied together so that the use of a jumper to reroute the signal is unnecessary. This is done through the use of the **INC** pin.

INC pins, by definition are "internally not connected" and may be used for routing of signals. Certain Pentium OverDrive processor **INC** pins should be connected to the signals that correspond to the Write-Back Enhanced IntelDX2 processor write back signals and the **SRESET** signal. Table 10-4 details pins that should be routed together. Please note that the last two columns in Table 10-4 are the pins on the Pentium OverDrive socket which must be routed together.

Table 10-4. Single Socket Compatibility Signals

Signal	Write-Back Enhanced IntelDX2 Processor Signal Pin	Pentium® OverDrive® Processor Signal Pin	Pentium® OverDrive® Processor INC Pins
INV	A10	N1	B11
HITM#	A12	U1	B13
CACHE#	B12	G1	C13
WB/WT#	B13	T1	C14
INIT	C10	F19	D11
FERR#	C14	B14	D15

Figure 10-1 below shows an example of how the INC pins shown in Table 10-4 should be connected together to allow single socket compatibility between the Write-Back Enhanced IntelDX2 processor and the Pentium OverDrive processor. The figure is provided as an example only and is not intended to be guide for how the signals should actually be routed on a motherboard.

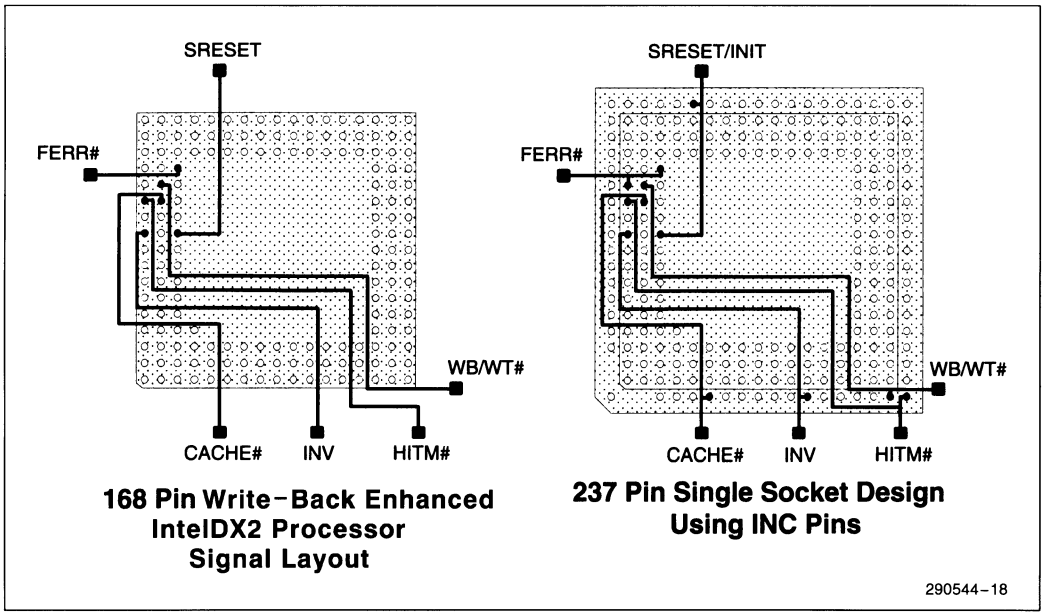


Figure 10-1. Sample Routing of INC Pins

10.2 Functional Differences

The Pentium OverDrive processor and the Write-Back Enhanced IntelDX2 processor have been designed to be functionally alike, but because the Pentium OverDrive processor is based on the advanced Pentium processor core, there are some minor differences that should be accounted for to ensure that a Pentium OverDrive processor will operate properly in a Write-Back Enhanced IntelDX2 processor-based system.

10.2.1 WRITE BACK PROCESSOR CACHE CONSIDERATIONS

Both the Write-Back Enhanced IntelDX2 processor and the Pentium OverDrive processor support an internal write back processor cache. The Pentium OverDrive processor carries over the Pentium processor cache protocol which supports multiple processors in the same system. The Write-Back Enhanced IntelDX2 processor cache coherency protocol is designed for single processor systems and is a subset of the Pentium OverDrive processor MESI protocol. If implemented correctly, a system can be designed that will support both protocols without sacrificing functionality. The differences of the cache cycles between the two processors are described below in Table 10-5.

For any cache read cycle (read hit or line fill), the Pentium OverDrive processor behaves in the same manner as the Write-Back Enhanced IntelDX2 processor.

As detailed in the Table 10-5, the Pentium OverDrive processor allows cache transitions on write through cycles (write hits to 'S' state lines). If **PWT** is driven low, the processor will use the state of **WB/WT#** to determine the final state of the entire cache line, even if only part of the line was written out by the write through cycle. If **WB/WT#** is driven HIGH, the state of the line will be changed to the 'E' state. If driven LOW, the line will remain in the 'S' state. This differs from the Write-Back Enhanced IntelDX2 processor and its dedicated 'S' state which always enforces the write through properties of a line stored in the 'S' state. If a system allows regions of memory to be stored as write through only via the **WB/WT#** pin, and other memory regions are stored as write back lines, then **WB/WT#** must toggle properly to ensure that 'S' state lines are never changed to write back 'E' lines. If the cache is used in a write back mode only (linefills are never stored in the 'S' state), then there will be no cache coherency issues, but there can be a performance issue due to snoop hits with **INV** = LOW.

For external snoop hits into the cache, the Pentium OverDrive processor differs in behavior from the Write-Back Enhanced IntelDX2 processor only in external snoop hits that drive **INV** = LOW. As shown in Table 10-5, any time a snoop hit occurs with **INV** = LOW, the Pentium OverDrive processor will change the cache line state to 'S'. The Write-Back Enhanced IntelDX2 processor will allow lines defined as write back ('M' and 'E') to transition to the initial write back line state of 'E'. If the line started out in the 'S' state, the Write-Back Enhanced IntelDX2 processor will protect the write through status of the line by keeping it in the 'S' state. On the Pentium OverDrive processor, if a system design supports snoop cycles with INV = LOW, this could result in write back lines ('M' or 'E') being stored in a write through state ('S'). This will not cause memory coherency issues, but any time a write cycle to the line is generated, the cycle will be driven to the bus, rather than simply stored in the cache in the 'M''

Table 10-5. Differences in Cache Cycles

Type of Cycle	Pentium® OverDrive® Processor Line State Transition	Write-Back Enhanced IntelDX2 Processor Line State Transition	Comments
Cache Write Hit to 'S' State Line	'S' to 'E' OR 'S' to 'S'	'S' to 'S'	The Pentium OverDrive processor samples **WB/WT#** on write through cycles if **PWT** is LOW to determine what kind of transition should occur.
External Snoop Hit **INV** = 0	'M' to 'S' 'E' to 'S' 'S' to 'S'	'M' to 'E' 'E' to 'E' 'S' to 'S'	The assumption that a Write-Back Enhanced IntelDX2 processor will operate in a single processor system allows for direct transitions to the 'E' state.

state. To avoid performance issues, systems that can drive **INV** = LOW should drive **WB/WT#** = HIGH when a write through cycle to such a line occurs on the bus. As shown in Table 10-5, this will ensure that a write back line that has accidentally been converted to a write through line will not cause more than one unnecessary write cycle on the bus.

10.2.2 STANDARD/ENHANCED BUS DIFFERENCES

Both the Write-Back Enhanced IntelDX2 processor and the Pentium OverDrive processor use the **WB/WT#** pin as an initialization input on the falling edge of **RESET.** Several signals behave differently depending on if the processors are operating in enhanced bus mode or standard bus mode. Some of these behaviors are slightly different between the Pentium OverDrive processor and the Write-Back Enhanced IntelDX2 processor, and are listed below in Table 10-6.

Table 10-6. Differences in Bus Modes

Functionality	Pentium® OverDrive® Processor	Write-Back Enhanced IntelDX2 Processor
Standard Bus Mode CPUID	0153xh x = 0 to F	0043xh x = 0 to F
Enhanced Bus Mode CPUID	0153xh x = 0 to F	0047xh x = 0 to F
Standard Bus Mode **INIT**	**INIT** is treated as an Interrupt	SRESET is not an interrupt
Standard Bus Mode **FLUSH#**	**FLUSH#** will take about 15 Bus CLKs No Write Backs	**FLUSH#** will take 1 Bus CLK No Write Backs

One item to note in Table 10-6 is that the **INIT** pin on the Pentium OverDrive processor is treated as an edge triggered interrupt in both the standard and enhanced bus modes. This means that **INIT** will not be recognized until instruction boundaries, and after **INIT** has been asserted and recognized, more ADS# cycles can be started, even if **INIT** has not been deasserted.

10.2.3 SOFTWARE DIFFERENCES

Due to the Pentium processor features found on the Pentium OverDrive processor, there are several software visible differences that should be accounted for in any system specific firmware or BIOS routines.

10.2.3.1 Cache Testing and Test Registers

The cache of the Pentium OverDrive processor is structured as separate code and data caches, each 16 KBytes in size. Because of this structure, the Pentium OverDrive processor supports Model Specific Registers (MSR's) for cache testing, rather than the Write-Back Enhanced IntelDX2 processor Test Registers. Any attempt to access the Write-Back Enhanced IntelDX2 processor test registers on the Pentium OverDrive processor will result in invalid opcode exceptions. For more information on testing the caches of the Pentium OverDrive processor, please contact Intel.

10.2.3.2 Timing Loops

Timing loops (i.e.: executing a tight loop that does nothing) are a common method of providing a software based delay for I/O recovery. Because of the Pentium processor core and an increased core speed, the Pentium OverDrive processor will be able to execute instructions must faster than previous generations of processors. It is suggested that timing loops be avoided, and that a hardware based delay scheme be developed, such as writing to a dummy I/O port that will delay the returning of **RDY#** for a fixed amount of time.

10.2.4 EXTERNAL SNOOPING REQUIREMENTS ON EADS#

The specification set out in the Hardware Design Considerations Section (Sections 4.1.1 and 4.1.2) must be observed to ensure that EADS# will be recognized properly by both the Pentium OverDrive processor and the Write-Back Enhanced IntelDX2 processor.

10.2.5 DIFFERENCES IN STOP GRANT STATE OPERATION

If the **STPCLK#** pin is asserted and the Pentium OverDrive processor issues the stop grant special cycle, the processor is in the stop grant state. While in this state, the following conditions apply:

1) If any of the following interrupts are asserted, they will be latched and serviced as soon as the **STPCLK#** pin is released and the processor exits the stop grant state:

   FLUSH#, SMI#, NMI, INIT

   If an interrupt is asserted and then released while the processor is in the stop grant state, it will be recognized once the processor exits the stop grant state even though the interrupt may be deasserted. This behavior is different than that of the Write-Back Enhanced IntelDX2 processor, which requires these interrupts to be held until the processor has exited the stop grant state.

   NOTE:
   INTR is a level triggered interrupt and will not be latched. It must be held until the interrupt acknowledge cycle to guarantee recognition.

2) Unlike the Write-Back Enhanced IntelDX2 processor, if **INIT** is asserted while in the stop grant state, the processor will not automatically exit the stop grant state and perform the **INIT.** As mentioned above, **INIT** is latched and will be recognized once the processor exits the stop grant state when **STPCLK#** is deasserted.

11.0 DC/AC SPECIFICATIONS

The electrical specifications in this section represent the electrical interface of the Pentium OverDrive processor. The Pentium OverDrive processor will be compatible to the AC/DC specifications presented in this section.

Table 11-1 provides the absolute maximum ratings. It is a stress rating only, and functional operation at the maximums is not guaranteed. Function operating conditions are given in Section 11.1 (DC Specifications) and 11.2 (A. C. Specifications).

Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the Pentium OverDrive processor contains protective circuitry to resist damage from static electric discharge, always take precautions to avoid high static voltages or electric fields.

Table 11-1. Absolute Maximum Ratings

Case Temperature under Bias . . . −30°C to +110°C

Fan/Heatsink Temperature under Bias . . . . . −5°C to +60°C

Processor Storage Temperature . . . . . −30°C to +125°C

Fan/Heatsink Storage Temperature . . . . . −40°C to +70°C

Voltage on any Pin with Respect to Ground . . −0.5V to (V_{CC} + 0.5V)

Supply Voltage with respect to V_{SS} . . . . . −0.5V to +6.5V

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

11.1 DC Specifications

Table 11-2 provides the DC operating conditions for the Pentium OverDrive processor.

Functional operating range: V_{CC} = 5V +5%; $T_{A(IN)}$ = 0°C to +55°C @33 MHz and 25 MHz.

Table 11-2. DC Parametric Values

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage	−0.3	+0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.3	V	
V_{OL}	Output Low Voltage		0.45	V	(Note 1)
V_{OH}	Output High Voltage	2.4		V	(Note 2)
I_{CC}	Power Supply Current CLK = 25 MHz CLK = 33 MHz		 1900 2800	mA	
I_{LI}	Input Leakage Current		±15	μA	(Note 3)
I_{IH}	Input Leakage Current		200	μA	(Note 4)
I_{IL}	Input Leakage Current		−400	μA	(Note 5)
I_{LO}	Output Leakage Current		±15	μA	
C_{IN}	Input Capacitance		13	pF	F_c = 1 MHz (6)
C_O	I/O or Output Capacitance		17	pF	F_c = 1 MHz (6)
C_{CLK}	CLK Capacitance		15	pF	F_c = 1 MHz (6)

NOTES:
1. This parameter is measured at:
   Address, Data, BEn 4.0 mA
   Definition, Control 5.0 mA
2. This parameter is measured at:
   Address, Data, BEn −1.0 mA
   Definition, Control −0.9 mA
3. This parameter is for inputs without pullups or pulldowns and $0 < V_{IN} < V_{CC}$.
4. This parameter is for inputs with pulldowns and V_{IH} = 2.4V.
5. This parameter is for inputs with pullups and V_{IL} = 0.45V.
6. Not 100% tested.

11.2 AC Specifications

Tables 11-3 and 11-4 provide the AC specifications for the Pentium OverDrive processor at external clock frequencies of 25 MHz and 33 MHz respectively. They consist of output delays, input setup requirements, and input hold requirements. All AC specifications are relative to the rising edge of the input system clock unless otherwise specified. Internal core frequencies will be a multiple of the system bus frequency.

11.2.1 V_{CC} TRANSIENT SPECIFICATION

Due to the on-board voltage regulator, the V_{CC} of the Pentium OverDrive processor is allowed to exceed the DC Voltage specifications (V_{CC} = 5V + 5%) when the processor creates a large current transient, as would be the case in a full operation to Autohalt transition (2.5A to 200 mA I_{CC} change). The width of the pulse that exceeds 5V + 5% should be no wider than 1ms, and can not exceed 5.5V. V_{CC} is not allowed to go below the DC specification of 5V − 5% at any time. This specification applies to the Pentium OverDrive processor only and can not be applied to any other Intel processors. Figure 11-1 shows an example of the V_{CC} transient specification.

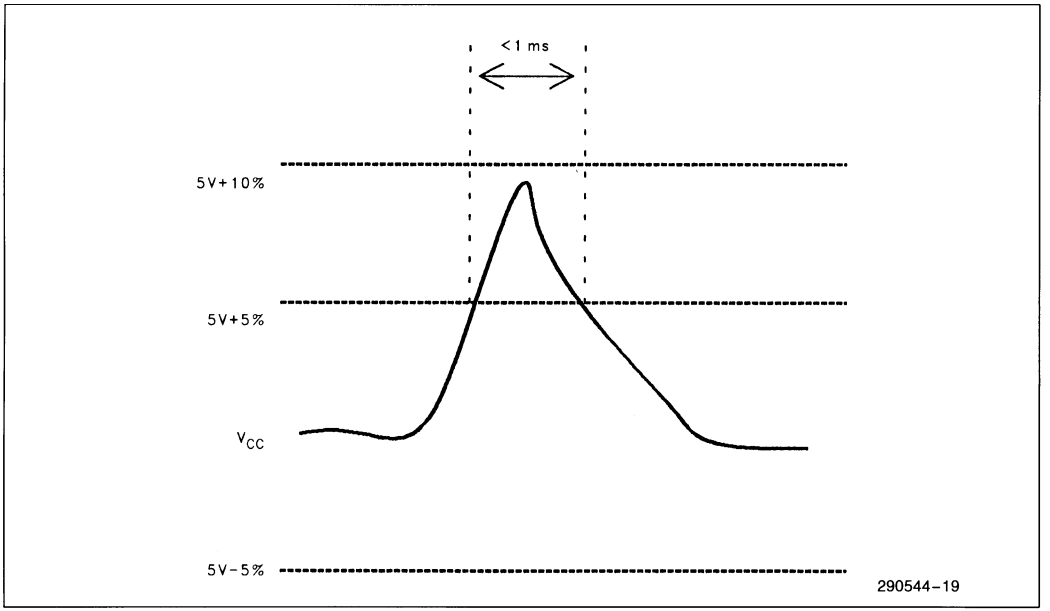


Figure 11-1. V_{CC} Transient Example

Table 11-3. Pentium® OverDrive® Processor—25 MHz AC Characteristics

V_{CC} = 5V + 5%; $T_{A(IN)}$ = 0°C to +55°C; C_L = 50 pF (1) Unless Otherwise Specified

Symbol	Parameter	Min	Max	Units	Figure	Notes
	Frequency	8	25	MHz		1X Clock Input to Processor
t_1	**CLK** Period	40	125	ns	10-1	
t_{1a}	CLK Period Stability		250	ps		Adjacent Clocks
t_2	**CLK** High Time	14		ns	10-1	at 2V
t_3	**CLK** Low Time	11		ns	10-1	at 0.8V
t_4	**CLK** Fall Time		4	ns	10-1	2V to 0.8V
t_5	**CLK** Rise Time		4	ns	10-1	0.8V to 2V
t_6	**A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK#, FERR#, BREQ, HLDA, SMIACT#,** Valid Delay	3	19	ns	10-3	
t_7	**A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK#** Float Delay		28	ns	10-3	After Clock Edge(2)
t_8	**PCHK#** Valid Delay	3	24	ns	10-3	
t_{8a}	**BLAST#, PLOCK#** Valid Delay	3	24	ns	10-3	
t_9	**BLAST#, PLOCK#** Float Delay		28	ns	10-3	After Clock Edge(2)
t_{10}	**D0–D31, DP0–3** Write Data Valid Delay	3	20	ns	10-3	
t_{11}	**D0–D31, DP0–3** Write Data Float Delay		28	ns	10-3	After Clock Edge(2)
t_{12}	**EADS#** Setup Time	8		ns	10-2	
t_{13}	**EADS#** Hold Time	3		ns	10-2	
t_{14}	**KEN#, BS16#, BS8#** Setup Time	8		ns	10-2	
t_{15}	**KEN#, BS16#, BS8#** Hold Time	3		ns	10-2	
t_{16}	**RDY#, BRDY#,** Setup Time	8		ns	10-2	
t_{17}	**RDY#, BRDY#,** Hold Time	3		ns	10-2	
t_{18}	**HOLD, AHOLD** Setup Time	8		ns	10-2	
t_{18a}	**BOFF#, SMI#** Setup Time	8		ns	10-2	
t_{19}	**HOLD, AHOLD, BOFF#, SMI#** Hold Time	3		ns	10-2	
t_{20}	**RESET, FLUSH#, A20M#, NMI, INTR, IGNNE#, INIT** Setup Time	8		ns	10-2	
t_{21}	**RESET, FLUSH#, A20M#, NMI, INTR, IGNNE#, INIT Hold Time**	3		ns	10-2	

Table 11-3. Pentium® OverDrive® Processor—25 MHz AC Characteristics (Continued)
V_{CC} = 5V + 5%; $T_{A(IN)}$ = 0°C to +55°C; C_L = 50 pF (1) Unless Otherwise Specified (Continued)

Symbol	Parameter	Min	Max	Units	Figure	Notes
t_{22}	**D0–D31, DP0–3, A4–A31** Read Setup Time	5		ns	10-2	
t_{23}	**D0–D31, DP0–3, A4–A31** Read Hold Time	3		ns	10-2	
t_{38}	**WB/WT#** and **EWBE#** Setup Time	8		ns	10-2	
t_{39}	**WB/WT#** and **EWBE#** Hold Time	3		ns	10-2	
t_{40}	**INV Setup Time**	8		ns	10-2	
t_{41}	**INV** Hold Time	3		ns	10-2	
t_{42}	**HIT#, HITM#** Valid Delay	3	19	ns	10-3	
t_{43}	**HIT#, HITM#** Float Delay		28	ns	10-3	Only during Three State Test Mode
t_{44}	**CACHE#** Valid Delay	3	19	ns	10-3	
t_{45}	**CACHE#** Float Delay		28	ns	10-3	
t_{46}	**STPCLK#** Setup Time	5		ns	10-2	
t_{47}	**STPCLK#** Hold Time	3		ns	10-2	

NOTES:
1. All timing specifications assume C_L = 50 pF. Section 9.2.1 provides the charts that may be used to determine the delay due to derating, depending on the lumped capacitive loading, that must be added to these specification values.
2. Not 100% tested, guaranteed by design characterization.

Table 11-4. Pentium® OverDrive® Processor—33 MHz AC Characteristics

V_{CC} = 5V + 5%; $T_{A(IN)}$ = 0°C TO +55°C; C_L = 50 pF (1) Unless Otherwise Specified

Symbol	Parameter	Min	Max	Units	Figure	Notes
	Frequency	8	33	MHz		1X Clock Input to Processor
t_1	**CLK** Period	30	125	ns	10-1	
t_{1a}	**CLK** Period Stability		250	ps		Adjacent Clocks
t_2	**CLK** High Time	11		ns	10-1	At 2V
t_3	**CLK** Low Time	8		ns	10-1	At 0.8V
t_4	**CLK** Fall Time		3	ns	10-1	2V to 0.8V
t_5	**CLK** Rise Time		3	ns	10-1	0.8V to 2V
t_6	**A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK#, FERR#, BREQ, HLDA, SMIACT#,** Valid Delay	3	14	ns	10-3	
t_7	**A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK# BP3, BP2,** Float Delay		20	ns	10-3	After Clock Edge(2)
t_8	**PCHK#** Valid Delay	3	14	ns	10-3	
t_{8a}	**BLAST#, PLOCK#** Valid Delay	3	14	ns	10-3	
t_9	**BLAST#, PLOCK#** Float Delay		20	ns	10-3	After Clock Edge(2)
t_{10}	**D0–D31, DP0–3** Write Data Valid Delay	3	14	ns	10-3	
t_{11}	**D0–D31, DP0–3** Write Data Float Delay		20	ns	10-3	After Clock Edge(2)
t_{12}	**EADS#** Setup Time	5		ns	10-2	
t_{13}	**EADS#** Hold Time	3		ns	10-2	
t_{14}	**KEN#, BS16#, BS8#** Setup Time	5		ns	10-2	
t_{15}	**KEN#, BS16#, BS8#** Hold Time	3		ns	10-2	
t_{16}	**RDY#, BRDY#,** Setup Time	5		ns	10-2	
t_{17}	**RDY#, BRDY#,** Hold Time	3		ns	10-2	
t_{18}	**HOLD, AHOLD** Setup Time	6		ns	10-2	
t_{18a}	**BOFF#, SMI#** Setup Time	7		ns	10-2	
t_{19}	**HOLD, AHOLD, BOFF#, SMI#** Hold Time	3		ns	10-2	
t_{20}	**RESET, FLUSH#, A20M#, NMI, INTR, IGNNE#, INIT** Setup Time	5		ns	10-2	
t_{21}	**RESET, FLUSH#, A20M#, NMI, INTR, IGNNE#, INIT** Hold Time	3		ns	10-2	

Table 11-4. Pentium® OverDrive® Processor—33 MHz AC Characteristics (Continued)
V_{CC} = 5V + 5%; $T_{A(IN)}$ = 0°C TO +55°C; C_L = 50 pF (1) Unless Otherwise Specified (Continued)

Symbol	Parameter	Min	Max	Units	Figure	Notes
t_{22}	**D0–D31, DP0–3, A4–A31** Read Setup Time	5		ns	10-2	
t_{23}	**D0–D31, DP0–3, A4–A31** Read Hold Time	3		ns	10-2	
t_{38}	**WB/WT#** and **EWBE#** Setup Time	5		ns	10-2	
t_{39}	**WB/WT#** and **EWBE#** Hold Time	3		ns	10-2	
t_{40}	**INV** Setup Time	5		ns	10-2	
t_{41}	**INV** Hold Time	3		ns	10-2	
t_{42}	**HIT#, HITM#** Valid Delay	3	14	ns	10-3	
t_{43}	**HIT#, HITM#** Float Delay		20	ns	10-3	Only during Three State Test Mode
t_{44}	**CACHE#** Valid Delay	3	14	ns	10-3	
t_{45}	**CACHE#** Float Delay		20	ns	10-3	
t_{46}	**STPCLK#** Setup Time	5		ns	10-2	
t_{47}	**STPCLK#** Hold Time	3		ns	10-2	

NOTES:
1. All signal timings except Boundary Scan timing specifications assume C_L = 50 pF. Section 9.2.1 provides the charts that may be used to determine the delay due to derating, depending on the lumped capacitive loading, that must be added to these specification values.
2. Not 100% tested, guaranteed by design characterization.

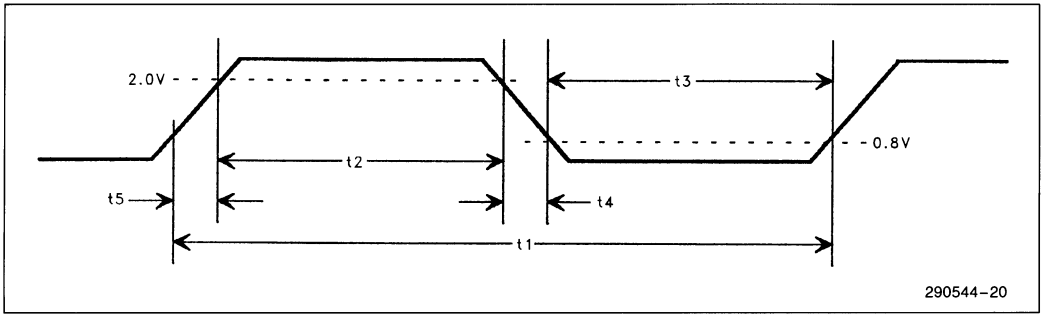


Figure 11-2. CLK Waveform

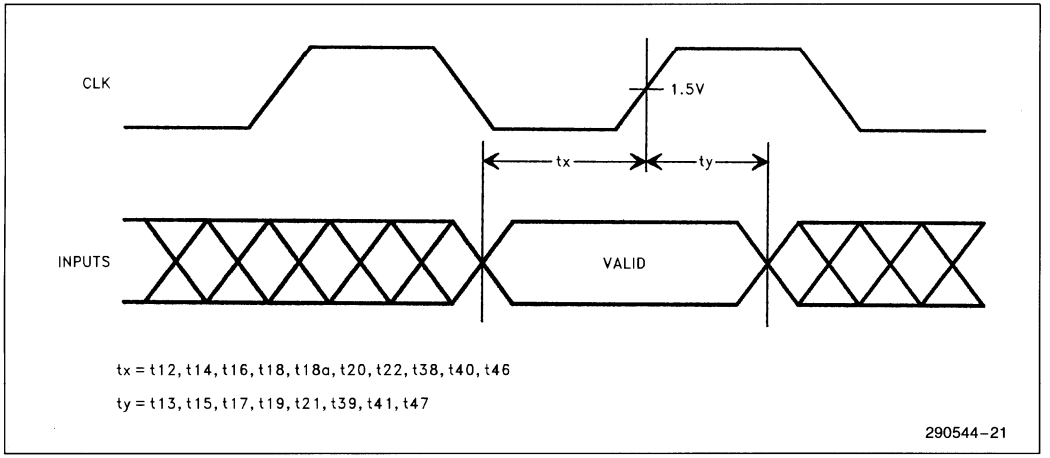


Figure 11-3. SETUP and HOLD Timings

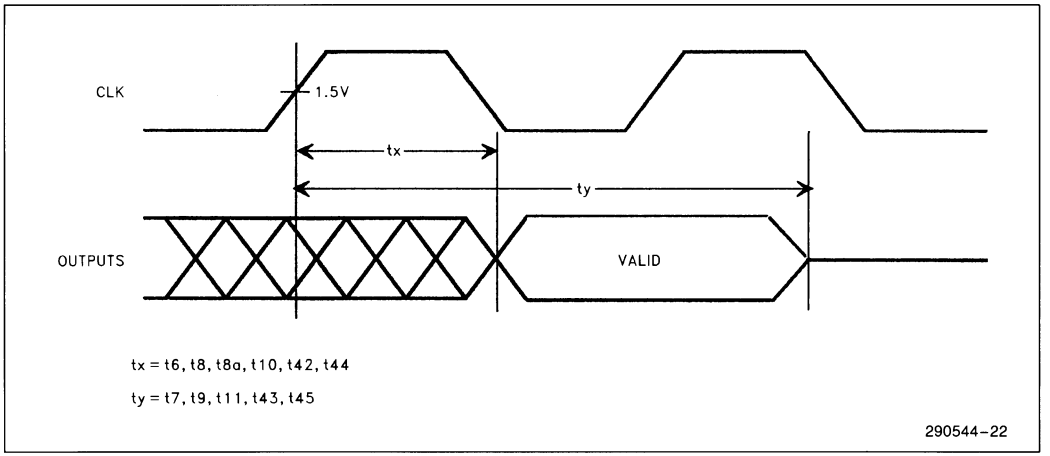


Figure 11-4. Valid and Float Delay Timings

11.2.2 DERATING I/O SPECIFICATIONS

Figures 11-5 and 11-6 can be used to determine the amount of derating necessary for a given amount of lumped capacitive load. This delay due to derating must be added accordingly to the specification values listed in Tables 11-3 and 11-4 for the Pentium OverDrive processor. These values are design estimates.

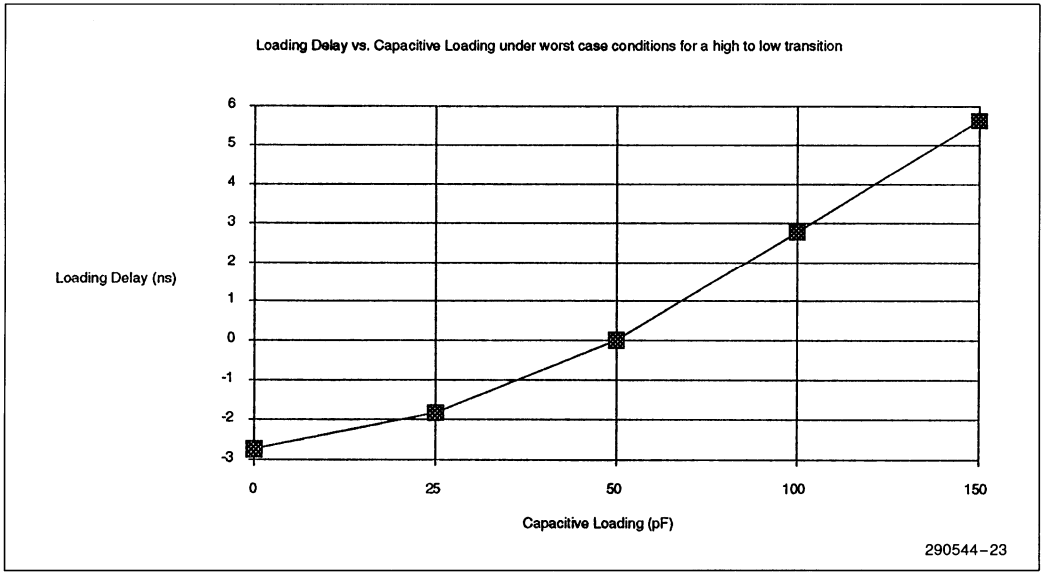


Figure 11-5. Loading Delay vs Load Capacitance (High to Low Transition)

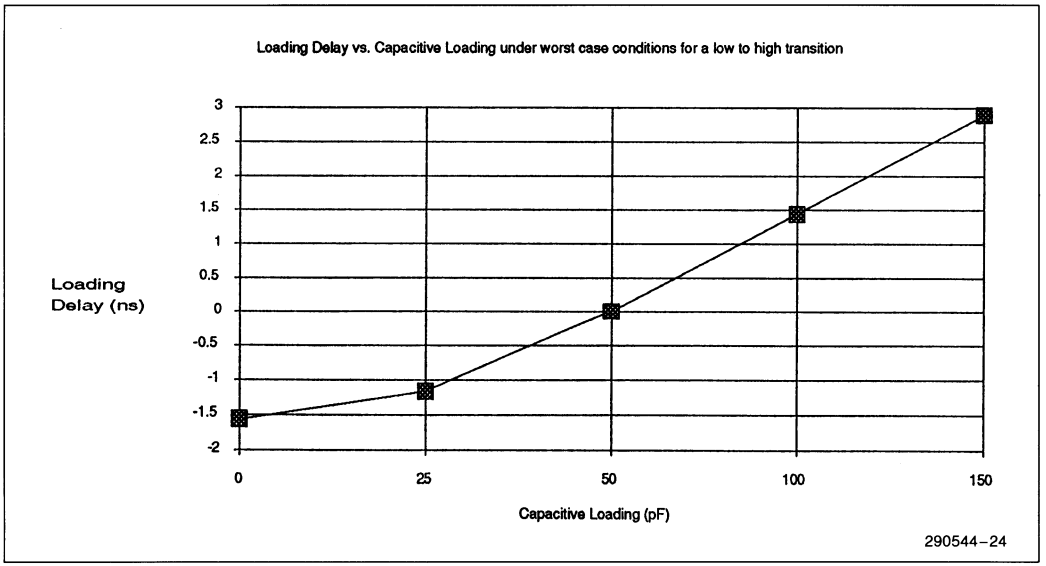


Figure 11-6. Loading Delay vs Load Capacitance (Low to High Transition)

Refer to the Pentium Processor Data Book for more information on instruction execution timing and pairing.

A generic discussion on the operation of cache memories can be found in the Intel Cache Tutorial available from your Intel sales representative or from Intel's Literature department, order #296543-002.

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